New Features in Version 14 of the Ampsa ADW

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Version 14 is a major Amplifier Design Wizard upgrade. Some of the main upgrades are listed below.

1. All the load-pull and synthesis features provided previously for Class-B power stages were generalized for Class-F, inverse Class-F and Ampsa Class-B2 operation too.

   Class-B2 is a new Ampsa class of operation with higher output power and efficiency than a Class-B stage with the same *I*/*V*-curve load-line boundary constraints. The high breakdown-voltage provided by GaN transistors are exploited in this class of operation to provide more power and higher efficiency than possible with a Class-B stage.

   In the continuous classes, the higher breakdown voltage is used to allow for reactive fundamental-frequency load lines, with the power and efficiency identical to the Class-B case. This is supposed to ease designing of the matching networks required, but this does not necessarily bear out in practice, especially with the demands placed on the compensating harmonic terminations.

   Moderate second-harmonic and third-harmonic terminations are required for Class-B2 operation (intrinsic opens or shorts are not required). Designing matching networks for this class of operation is generally easier than doing so for the other classes.

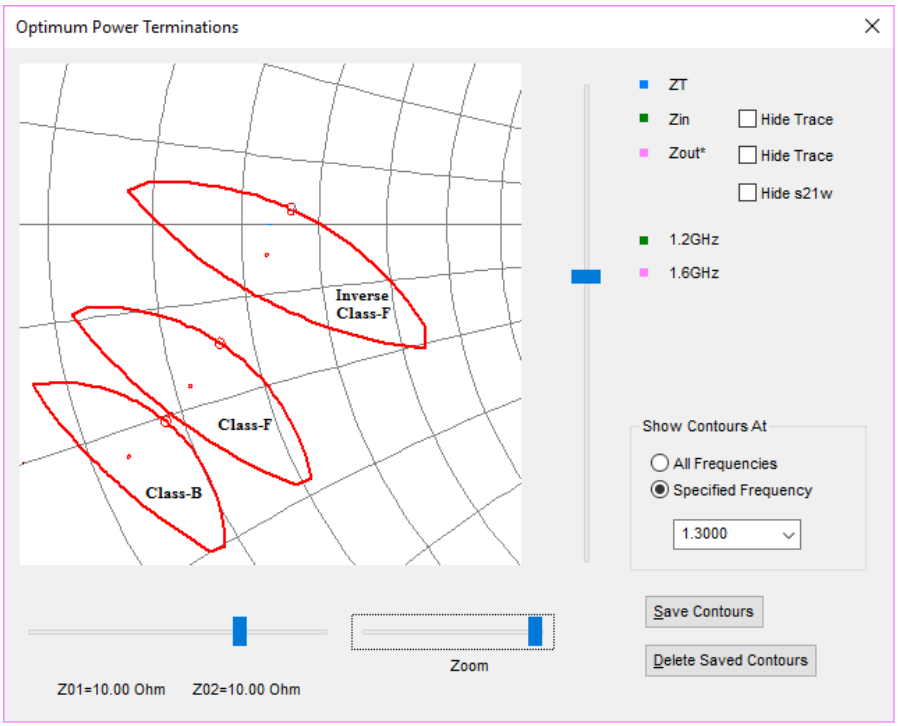

Figure 1. Ampsa ADW constant power contours for Class-B, Class-F and inverse Class-F operation are compared here. The highest efficiency point on each contour is marked. Note that the contours were generated by using a linear model for the transistor (Extended Cripps [1, 2] approach).

In the ADW, matching networks can be designed to control the power performance of an amplifier stage by using constant power contours and/or by controlling the intrinsic load terminations directly. (Power parameters [3] are used to map the intrinsic load line to input impedance required from the load matching network.) These two approaches can also be combined by first using the CIL wizard power contour option to select the fundamental-frequency load lines to be targeted, followed by using the intrinsic load-line option to add harmonic constraints to the fundamental-frequency matching problem.

The fundamental-frequency load lines in the CIL power contour section are calculated under the assumption that the ideal harmonic terminations for the class investigated are in place.

ADW power contours for Class-B, Class-F and inverse Class-F operation are compared in Figure 1. The power levels targeted are similar and the number of harmonics were restricted to three. The highest efficiency point on each contour is marked.

Ampsa Class-B2 and inverse Class-F power contours are compared in Figure 2. The power levels targeted were 0.5 dBm below the maximum for each class. In this example, the maximum power level for Class-B2 is 1 dBm below that of inverse Class-F. The number of harmonics were not restricted.

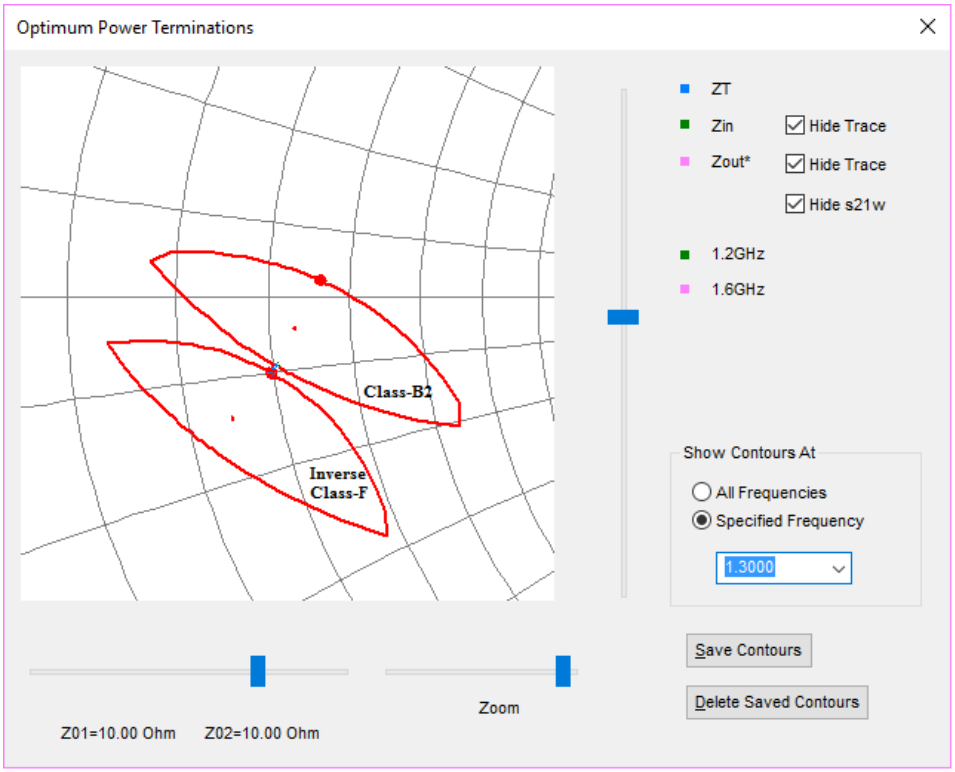

Figure 2. Class-B2 and inverse Class-F constant power contours are compared here (The power levels targeted are 0.5 dBm below the respective maximum power levels and the number of harmonics allowed were not restricted).

Better efficiency can usually be obtained by targeting power levels below the maximum possible (Some power is sacrificed for improved efficiency). The highest efficiency points on the power contours targeted can be selected automatically. The points to be targeted can be saved for use in the intrinsic load-line section by using the Save Z_{Li} option provided on the Summary page of the CIL wizard (refer to Figure 3).

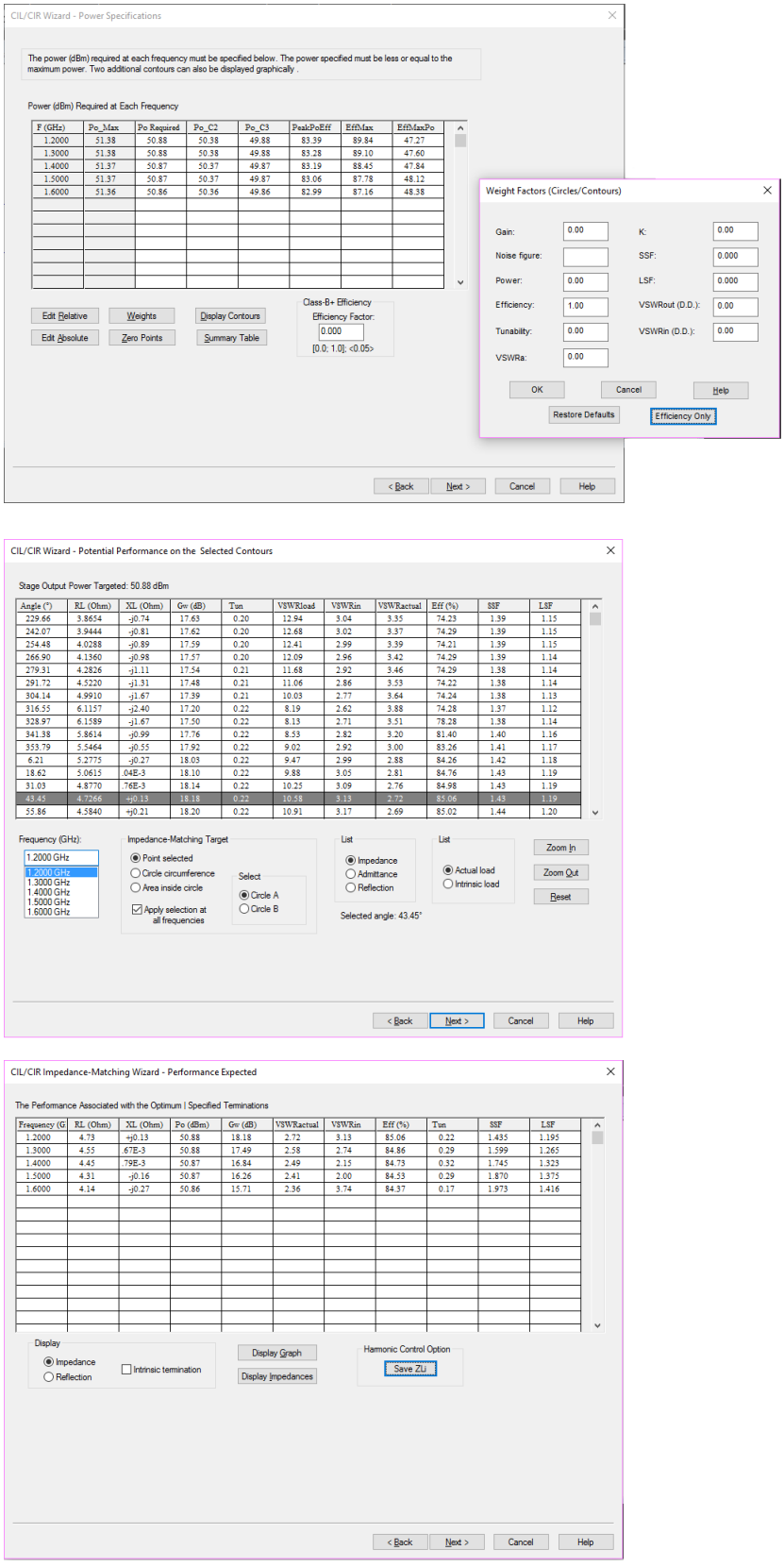

Figure 3. The Weights command on the Power Specifications CIL wizard page can be used to set the error function to target the highest efficiency point on each power contour selected automatically. The Save Z_{Li} command provided on the Summary page can be used to save the fundamental-frequency load terminations targeted for use in the intrinsic load-line section of the CIL wizard.

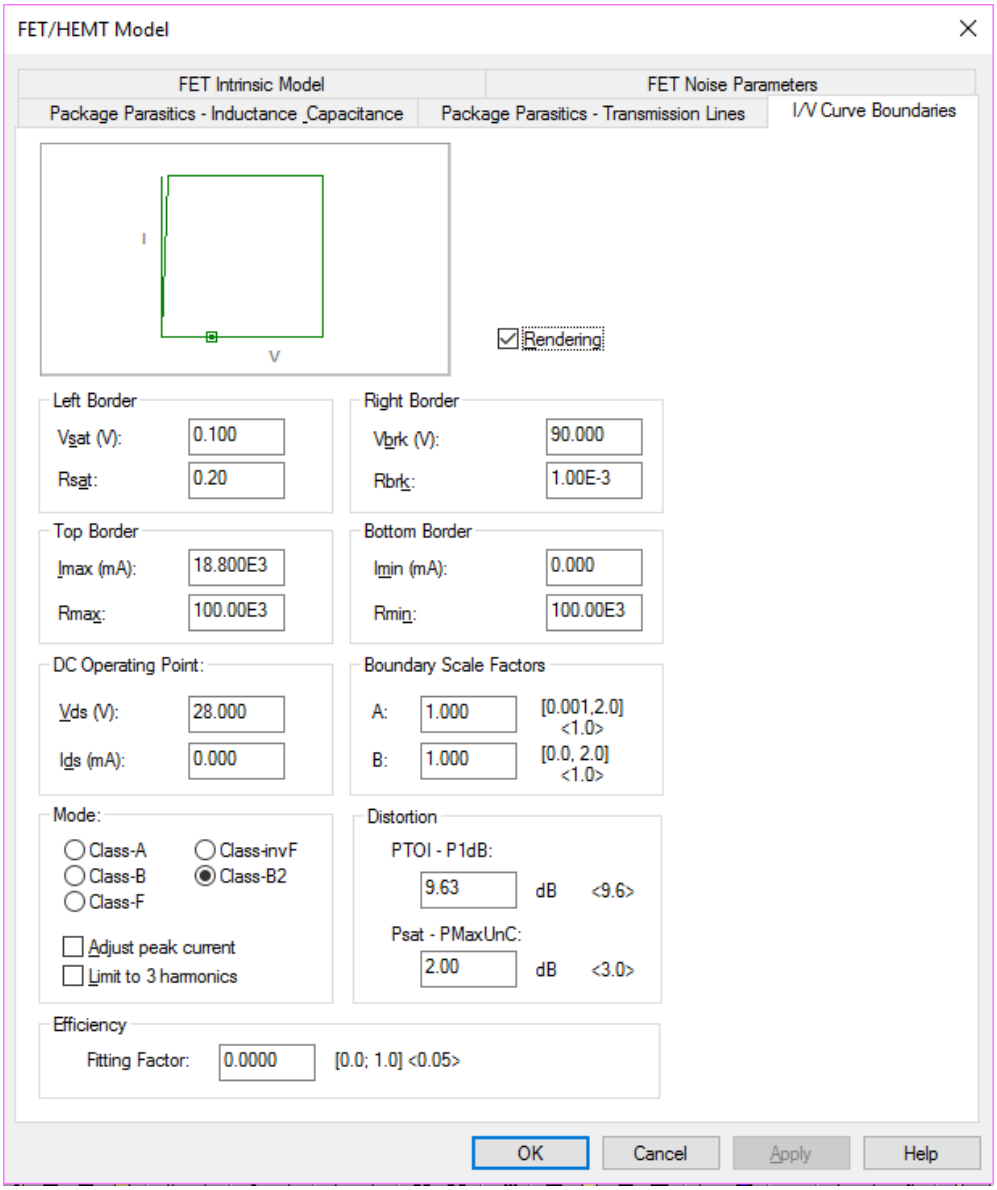

Figure 4. The Version 14 *I*/*V*-curve boundaries wizard page provided when a model is fitted to a transistor.

2. More power can be obtained from a Class-F stage (square-wave voltage; half-sinusoidal current) or inverse Class-F stage (square-wave current; half-sinusoidal voltage) than from a Class-B stage (sinusoidal voltage; half-sinusoidal current) with the same intrinsic *I*/*V*-curve boundary line constraints. (The boundaries apply to the instantaneous intrinsic output voltage and current.) The option to trade the potentially higher power for a higher impedance fundamental-frequency load line (easier to match) is provided on the *I*/*V*-curve boundaries wizard page (Adjust peak current option in Figure 4). The option to constrain the number of harmonics in the relevant waveforms to three is also provided (Limit to 3 harmonics option).

   Note that the efficiency of an inverse Class-F stage is reduced more than that of a Class-F stage when the harmonics are restricted (81.6% maximum versus 90.7% when three harmonics are allowed).

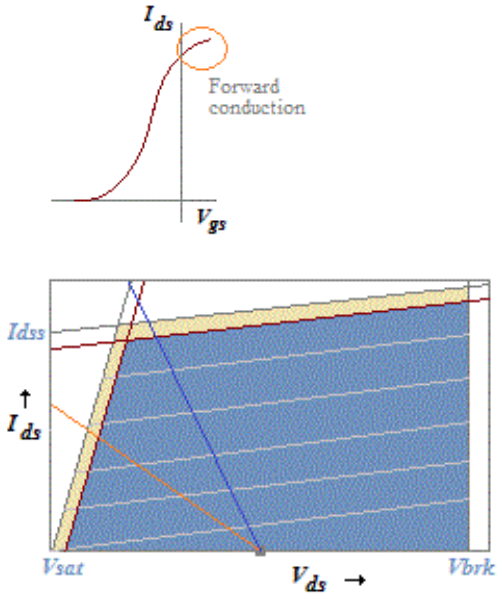

Figure 5. Less distortion can be expected as the allowable intrinsic load-line area is moved away from the ohmic region and the forward conduction region. The blue Class-B load-line shown is current limited, while the orange load-line is voltage limited.

3. The transistor load-line boundaries lines in the ADW are usually set for maximum power and maximum efficiency. When linear operation is required, clipping of the waveforms and forward conduction of the gate are not desirable (the intermodulation distortion increases sharply with clipping or forward conduction). The boundaries can be adjusted manually for this purpose or the boundary scale factors provided on the *I*/*V*-curves boundaries wizard page can be used.

   When the second scale factor (*B*) in Figure 4 is set to zero, all the fundamental-frequency boundaries are adjusted with the same scale factor (*A*). (The fundamental-frequency boundaries are not the same as the boundaries for the instantaneous voltage and current.) The boundaries are adjusted to scale the swing in the fundamental-frequency voltage and current with the factor specified. If the scaling is adequate, clipping will be reduced and forward-conduction will be eliminated, with improved linearity, but reduced power levels and efficiency.

   The effect of interaction with the ohmic/knee area (voltage clipping) can be expected to be different from the effect of approaching the forward conduction area (current clipping), and asymmetrical scaling of the maximum fundamental-frequency voltage swing and current swing allowed may lead to better linearity with less penalty in power and efficiency. When both scale factors are non-zero (bigger than 0.001), the maximum allowed fundamental-frequency voltage swing is scaled with *A* and the maximum allowed fundamental-frequency current swing is scaled with *B*. Some experimentation is generally required to find the best scale factors for the degree of linearity required.

   When both scale factors are 1.0, or when *A*=1.0 and *B*=0.0, the boundaries specified will not be modified.

   Note that the baseband intermodulation products at the input and the output of the transistor must be suppressed when the linearity is important. This implies low-impedance terminations at the gate and the drain at the baseband frequencies. Good suppression can usually be obtained by using coils or (RF) shorted lines with inductance just high enough to not disturb the passband

performance. Alternatively, a low-inductance inductor or a suitable shorted line can be used as the output-side or input-side element of the input or output matching network, respectively, with each matching network designed to absorb the effect of the inductor or line added.

When linear operation is required, the input voltage should not be excessive (This will result in significant second-harmonic generation by C_{gs} and may cause forward conduction of the gate). Presenting a low-impedance source termination to C_{gs} at the second harmonic is also advisable.

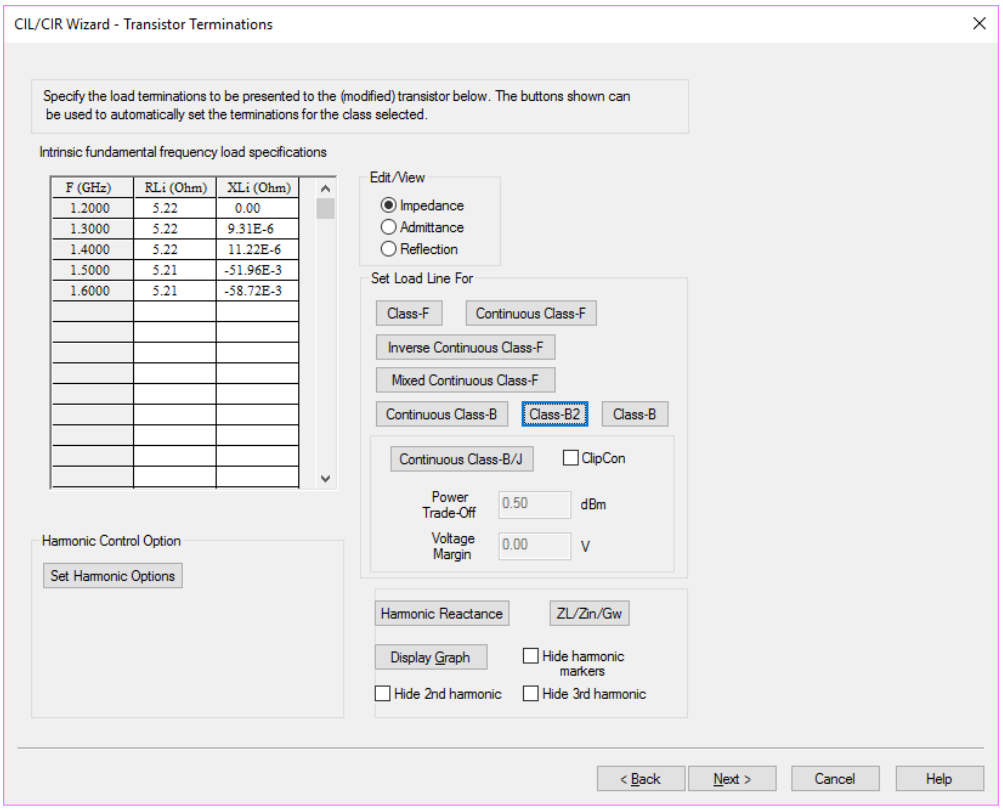

Figure 6. Class-B and Class-B2 options were added to the CIL wizard page for controlling the intrinsic load termination of a transistor.

4. The Intrinsic load-line of a transistor can be controlled directly by selecting to control the intrinsic load on the Power Module Options page of the CIL wizard. The options provided on the Terminations page (refer to Figure 6) were extended to provide control over the intrinsic load line of a Class-B2 stage too. A new Class-B command is also provided. Greater control over the Class-B harmonic terminations is possible with this option compared to using the Set Harmonic Options command.

   The Set Harmonic Options command can be used to control the harmonic terminations of Class-A, Class-B, Class-F and inverse Class-F stages. High-impedance or low-impedance harmonic terminations (approximate shorts or opens) are required for these stages. No preference is given to whether the approximate short or open is inductive or capacitive. This option does not apply to a Class-B2 stage.

   The continuous-mode commands should be used to control the intrinsic load terminations of the continuous classes [4 – 9]. The power parameters are used to map the intrinsic load-lines targeted to the input impedance required from the load matching network to be designed.

Note that the second-harmonic clipping contours introduced by Tanner, Tasker and Cripps [4] are also supported in the ADW. The minimum drain voltage targeted can be zero or can be set to a higher value to allow for the voltage knee or reduced interaction with the knee (Voltage margin set).

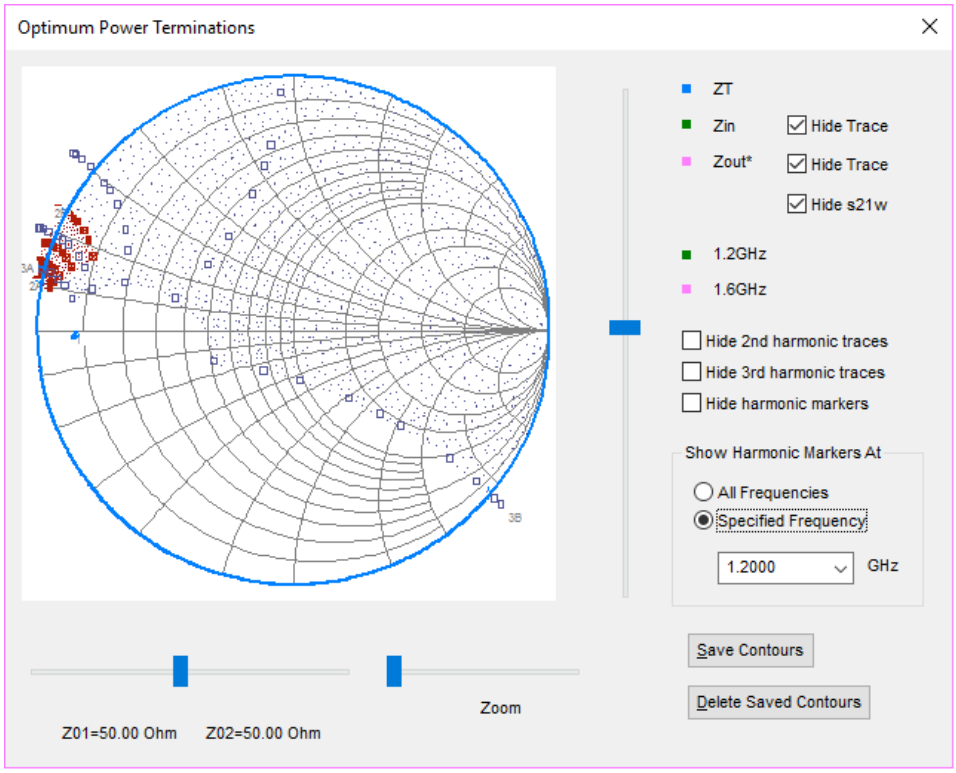

Figure 7. An example of the harmonic-frequency target areas for the external load terminations of a Class-B2 stage at a specific frequency. The red markers show acceptable load terminations for the second harmonic, while the blue markers are for the third harmonic. Note the overlap in the target areas in this example. While considerable harmonic resistance can be present at the insertion point for the matching network in the circuit, the intrinsic Q-factor ($|X_{Li} / R_{Li}|$) will still be larger than 4.0 in this example.

The harmonic reflection coefficients to be targeted should generally rotate clockwise on the Smith Chart with increasing frequency and the third-harmonic reflection coefficients should be located clockwise to the second-harmonic reflection coefficients. This behaviour is built into the Class-B2 specifications. Experimentation with the relevant design parameter is required to enforce this behaviour for the continuous classes. When the transistor parasitics are severe, it may not be possible to obtain the required behaviour for both the second and the third harmonic.

5. The Output Power page in the ADW optimization wizard was re-organized and a command was added to allow optimization of the harmonic terminations of a Class-B2 stage. The new page is shown in Figure 8.

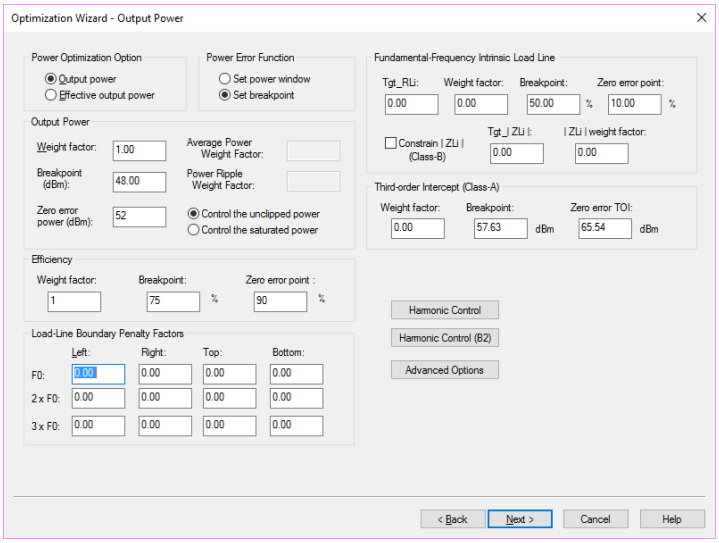

Figure 8. The Output Power page in the ADW optimization wizard was re-organized and a command was added to allow optimization of the harmonic terminations of a Class-B2 stage.

6. Microstrip step, T-junction and cross discontinuities can now be modelled in the ADW by using two-port, three-port or four-port *S*-parameters obtained from EM simulations of the respective discontinuities (refer to Figure 9). This capability is important in high power amplifier stages where the discontinuity effects can be severe and difficult to model over a large frequency range.

   An example of such a network is provided in Figure 10. The ADW input reflection coefficient for the network is compared to that obtained in an Axiem™ simulation in Figure 11. The difference without using the *S*-parameter models is significant. The *S*-parameters required for the microstrip discontinuities in the ADW were obtained from EM simulations in Sonnet®.

   The behaviour of the discontinuities should be considered up to at least the third harmonic, and preferably up to the fourth harmonic. If the discontinuity effects are not modelled accurately, the intrinsic harmonic terminations can be very different from those targeted.

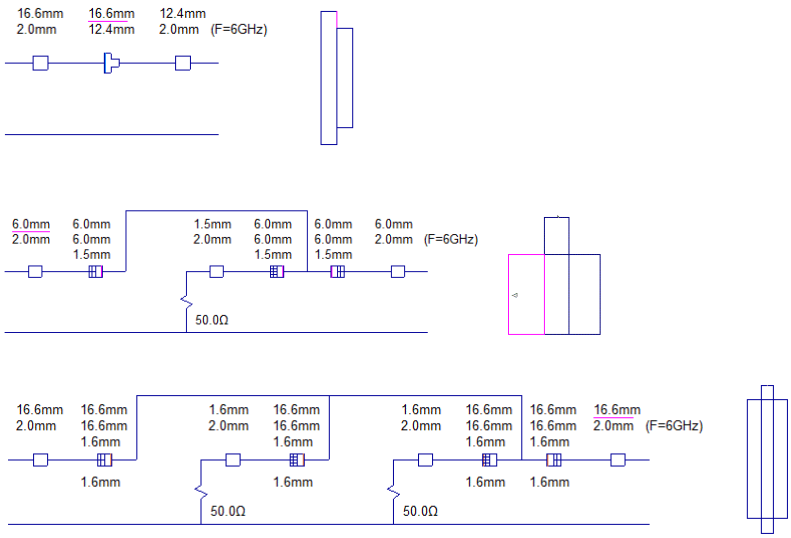

Figure 9. ADW schematics for an *S*-parameter based microstrip step junction, T-junction and cross junctions.

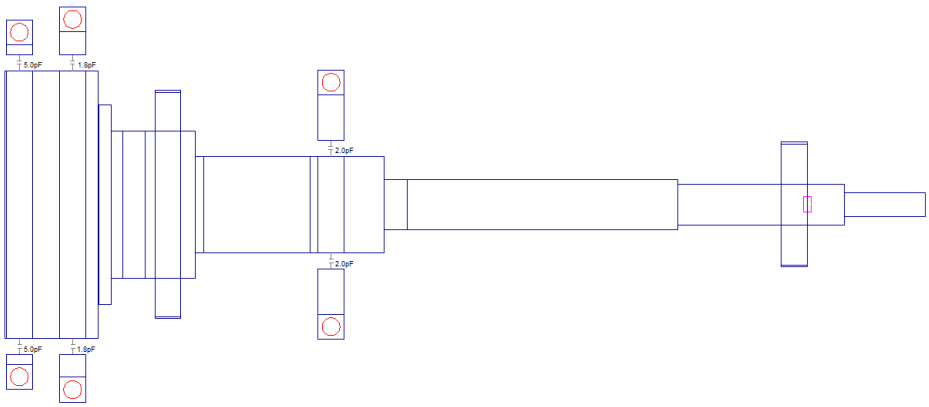

Figure 10. The artwork of an ADW matching network designed by using *S*-parameter based models for the microstrip junctions. The parasitic inductance specified for each capacitor was 0.3nH.

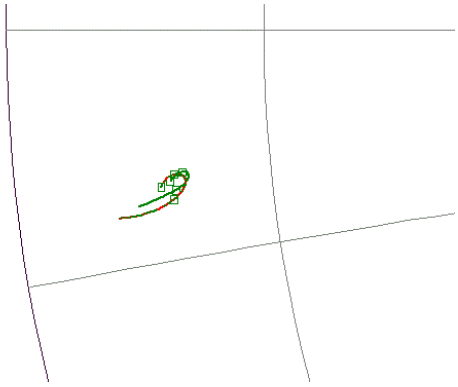

Figure 11. The ADW input reflection coefficients of the matching network in Figure 10 are compared to those obtained from an Axiem™ simulation. The *S*-parameters used to model the microstrip discontinuities in the ADW were obtained from EM simulations in Sonnet®.

Note that it is important to consider the actual circuit terminations to be presented to the amplifier stage at the harmonic frequencies. If these terminations are not known or will not remain constant, it is important to design networks to create a predictable harmonic environment. This could be done with harmonic traps or filters at strategic locations. The harmonic impedance to be presented to the matching network to be designed should be known at the design stage.

7. The power contours at up to four passband frequencies can be displayed simultaneously in the ADW (The lowest and highest passband frequencies and two frequencies inside the passband are selected automatically). Viewing all the contours simultaneously can be confusing and the option to limit the power contours to a single frequency is now also provided.

   The power contours (or the constant gain or constant noise figure circles) viewed can be saved for comparison with a different set of contours (see Figures 1, 2 and 12). Up to three sets of contours can now be saved. The same Smith Chart normalization impedance must be used for the contour sets to be compared.

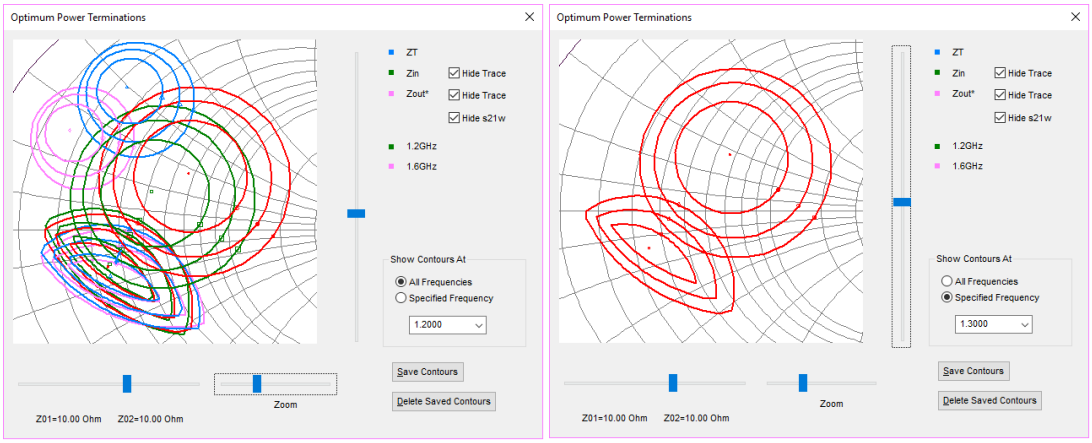

Figure 12. Constant transducer power gain circles are plotted with constant output power contours in this example.

References.

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