Ampsa ADW Stability Features

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Inherent or conditional stability of single-ended amplifiers can be ensured by using standard stability factors like the Rollette stability factor (*k*), the Sterne stability factor (*K*), *mu* [1] and *mu-prime* [1]. When transistors are connected in parallel or are combined with symmetrical combination networks, odd or even mode oscillations also become possible. Odd-mode oscillation conditions can fully escape detection by the standard stability factors when symmetrical combination networks are embedded in a larger network. Loop gain analysis or pole-zero techniques can be used to detect and eliminate the potential for odd-mode oscillations in amplifier circuits. The techniques used in the ADW to ensure stability in single-ended circuits and circuits with transistor combination networks are discussed below.

ADW Load and Source Stability Factors (*LSF* and *SSF*)

The Rollette stability factor (*k*), the Sterne stability factor (*K*) and generalized versions of the *mu* [1] and *mu-prime* [1] stability factors can be calculated in the ADW. The stabilizing influence of the terminations is included in the Sterne stability factor.

A circuit will be inherently stable if $k \geq 1$, and the magnitudes of s_{11} and s_{22} are smaller or equal to 1. (In the ADW, an exclamation mark is appended to the *k* value when the magnitude of one of the reflection parameters is bigger than 1.0). A circuit will also be inherently stable when *mu* > 1 and *mu-prime* > 1. (The one condition implies the other.) When a circuit is inherently stable, oscillations will not be possible with any passive termination and all the terminations inside the unit circle on the Smith Chart are allowed as source or load terminations.

Assuming arbitrary angles for the reflection coefficients, *mu* and *mu-prime* indicate how much the source or load impedance of a circuit can deviate from 50 Ohm (expressed as a reflection coefficient) before the circuit may become potentially unstable (negative input or output resistance).

The *SSF* (source stability factor) and the *LSF* (load stability factors) are generalized versions of *mu-prime* [1] and *mu* [1], respectively. The *SSF* is identical to *mu-prime* as defined in [1], and the *LSF* is identical to *mu* (as defined in [1]), when the terminations of the circuit are 50 Ohm. When the circuit terminations are complex, the values calculated will be different.

Assuming arbitrary angles for the reflection coefficients, positive values for *SSF* and *LSF* indicate how much the source or load impedance can deviate from the impedance targeted (expressed as complex normalized reflection coefficients) before the circuit may become potentially unstable (negative input or output resistance). The source | load reflection coefficients are calculated by using the conjugate of the actual (or targeted) source | load impedance as the normalization impedance for the source | load impedances considered.

When negative, the absolute value of *SSF* indicates the range of source reflection coefficients for which the output resistance will be negative (that is, assuming arbitrary angles for the source reflection coefficients). Outside the range defined, the output resistance could be positive or negative, depending on the angle of the reflection coefficient.

Similarly, when negative, the absolute value of *LSF* indicates the range of load reflection coefficient for which the input resistance will be negative (with arbitrary angles for the load reflection coefficients). Outside the range defined, the input resistance could be positive or negative, depending on the angle of the reflection coefficient.

The *SSF* or *LSF* is calculated by solving for the constant mismatch circle [2] which has a single intersect point with the relevant stability circle (see Figure 1). For potential stability, this mismatch circle must be located outside the stability circle. This will be the case when the relevant stability factor is bigger than zero.

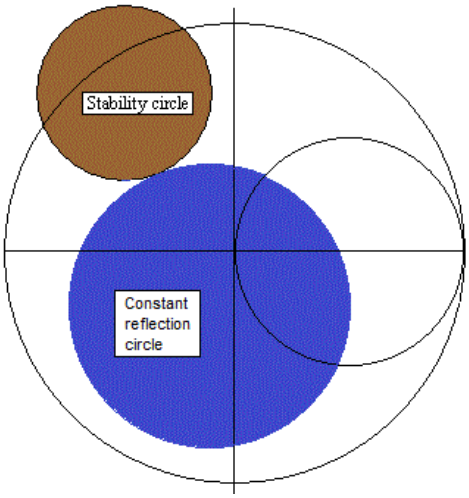


Figure 1. With arbitrary angles for the load reflection coefficients, the largest mismatch allowed in the load before a circuit may become potentially unstable (|*LSF*|, when *LSF* > 0.0) is calculated by solving for the constant mismatch circle which has a single intersect point with the load stability circle. For potential stability, this mismatch circle must be outside the stability circle.

When the Sterne stability factor is bigger than one, the circuit will be stable with the terminations in place. While this factor also indicates relative stability (that is, the stability increases as *K* increases), the *LSF* and *SSF* are direct measures of how much the selected load and source terminations may change before stability may become an issue. When the *LSF* or *SSF* is negative, the absolute value indicates how much the terminations must change before the associated input or output resistance may be positive.

Loop Gain Stability

The stability factors discussed above are black box stability factors – no structural information about the circuit analyzed is required or used. It is known that oscillations can occur in circuits with symmetrical combination sections for transistors when these factors indicate that the input and output impedance of the circuit will not have any negative resistance. The question arises as to how oscillating conditions are shielded from outside inspection in these circuits?

When the input impedance or output impedance of such a circuit is calculated, even-mode currents are assumed for the two symmetrical halves of the transistor combination loop (refer to Figure 2). However, odd-mode currents could be generated in the combination loop by oscillation (that is, if the conditions for oscillation are satisfied) and because of the symmetry, the odd-mode voltages at the combining nodes will be zero. The total voltage (super-position) at each of the combination nodes will, therefore, still be the even mode voltage. The currents flowing into the combination loop from the external circuitry will also remain the same as those calculated for the even mode. Because the effective voltages and currents did not change, the input impedance at the input combination node and the output impedance at the output combination node will, therefore, also still be the even mode impedance.

The two transistors are assumed to oscillate in anti-phase in the odd mode and in phase in the even mode. Note that the loop is not symmetrical when the oscillation conditions for each transistor are considered (forward transmission through one transistor and reverse transmission through the other).

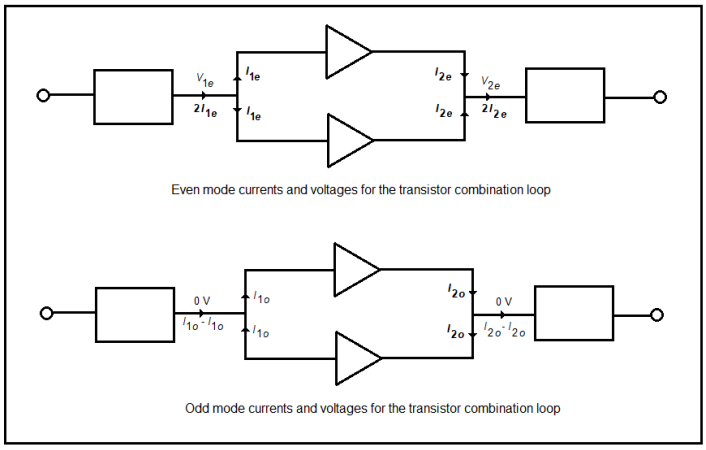


Figure 2. Odd-mode currents in a symmetrical combination section will not influence the input or output impedance of the section (pole-zero cancellations). Furthermore, if the loop is perfectly symmetrical, the circuit external to the loop does not affect the odd mode inside the loop.

It follows from the above that for amplifiers with symmetrical combination networks, *LSF* and *SSF* stability factors bigger than 1.0 may not be sufficient to ensure stability. The loop gain associated with each symmetrical combination section should also be calculated to ensure that odd or even mode oscillations cannot start in the loop. Note that the circuit external to the loop can improve the stability for the even mode but has no effect on the odd mode (that is, if the loop is perfectly symmetrical).

The number of potential oscillation modes increases with the number of combination loops. Stability should be ensured for all these modes. The modes to be considered when four transistors are combined are shown in Figure 3. Odd-mode oscillation is possible in the inner, as well as the outer loops.

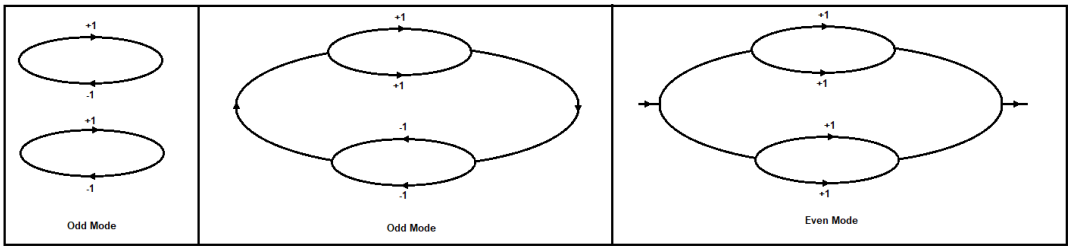
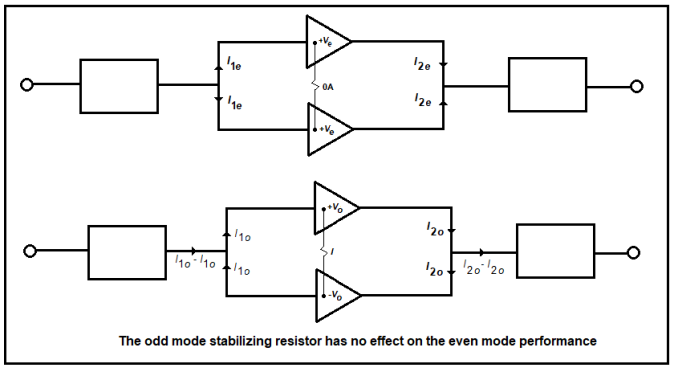


Figure 3. The modes to be considered when four transistors are combined (odd-mode oscillations in the inner loops, and even and odd modes in the outer loop).

A good approach (strongly recommended when possible) to designing stable symmetrical combination sections is to ensure that the two halves of the section are inherently stable before combining them. This will ensure positive open-loop resistance and better behaviour for the feedback loop. Negative resistance can still be generated inside the loop by the feedback.

Note that odd-mode stabilizing resistors can be added inside a symmetrical section to prevent odd-mode oscillations without degrading the even-mode performance (see Figure 4). The resistive loading sections added should be electrically short to have minimal effect on the even-mode performance.



The circuit external to the active loop can improve the stability for the even mode, but has no effect on the odd-mode if the loop is perfectly symmetrical. With some asymmetry, cancellation of the external currents will not be perfect, and the external circuit will have some effect on the odd mode in the loop.

Figure 4. Odd-mode stabilizing resistors can be used to minimize the effect of any odd-mode stabilization required on the performance.

Setting up a combination section (symmetrical or asymmetrical) for loop gain analysis in the ADW is illustrated in Figure 5. One half of the section is set up by adding an ISE block (input series cascade network) and an OSE block (output series cascade network) to the transistor, while the other half is set up as an ADW voltage-shunt feedback block.

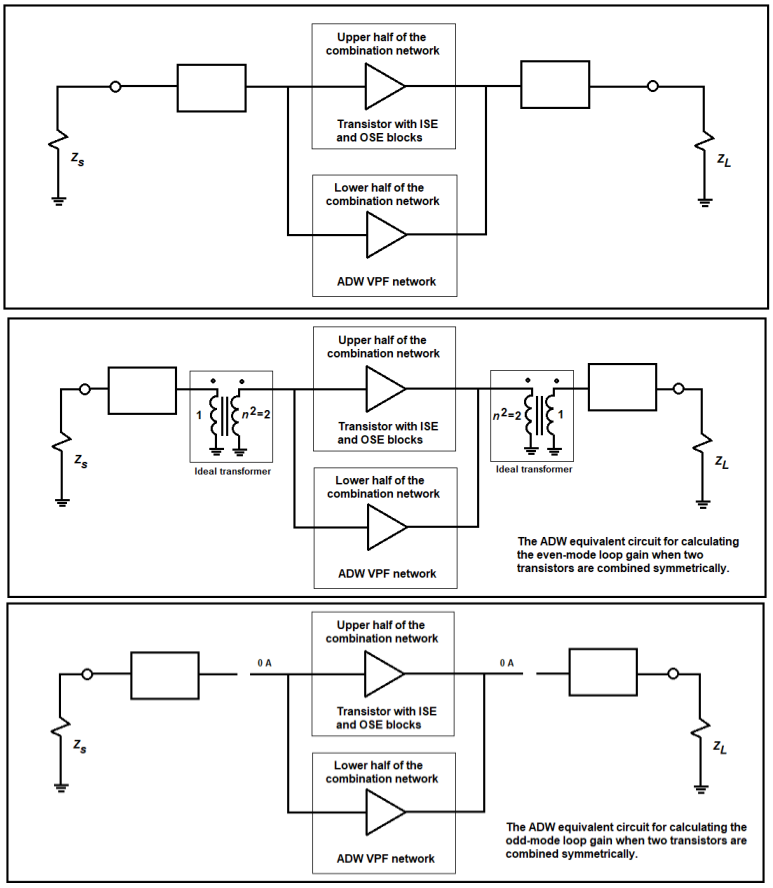


Figure 5. Setting up a symmetrical transistor combination section for loop-gain analysis in the ADW. The loop gain should be calculated for various combinations of possible circuit terminations (Z_s and Z_L). The circuit terminations do not affect the odd mode.

Loop gain analysis in the ADW assumes an active device in the main path and a passive network in the voltage-shunt feedback path. With active devices in both paths and symmetry, both transistors will oscillate. In the even mode, the oscillations will be in-phase and in the odd-mode in anti-phase. Assuming oscillation in only the main path, the impedances presented to the combining section by the

external circuitry must, therefore, be doubled for the even mode and set to open circuits for the odd mode (see Figure 5). No current flows from the combining section to the external circuity in the odd mode, and odd-mode oscillations will, therefore, not be dampened by the external circuitry.

Via-holes are often shared between adjacent transistors in a MMIC PA to save space. When this is done, an electrical connection is made between the source lines of the two transistors. This connection will have different effects on the even mode and the odd mode (see Figure 6). Because of the virtual ground associated with the odd mode, the odd-mode loop gain will increase when the connection is made. More stabilization may, therefore, be required for the odd mode when sources are connected.

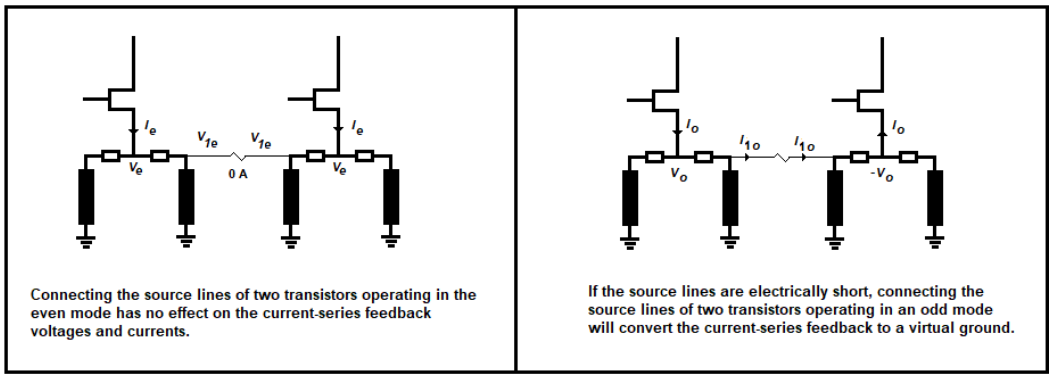


Figure 6. The effects on the even and the odd modes when an electrical connection is made between the source lines of two transistors.

With the circuit set up correctly, the ADW loop gain analysis command can be used to analyse the circuit. A Bode plot will be created for the magnitude and phase of the gain around the loop ($-\beta A$). The gain and phase margins can be obtained from the plot, when relevant. The loop gain should be calculated for all the circuits in Figure 5. If the circuit analyzed is not inherently stable, various combinations of possible circuit terminations (Z_s and Z_L) should be considered. The circuit terminations do not affect the odd mode.

It is important to verify the stability over the full range of *dc* currents expected in the transistors. The transistor gain generally increases with increasing current, with changes in the associated *S*-parameters.

Only odd-mode oscillating conditions fully escape the *LSF* and *SSF* stability measures. With the transformers in Figure 5 added, these measures are adequate for preventing even-mode oscillations. The fact that the odd mode is not affected by the circuit terminations, also simplifies controlling the stability. Inherent stability of the circuit and the even-mode equivalent of each combination loop, and adequate gain and phase margins for the odd-mode equivalent of each combination loop should be sufficient to ensure stability. Allowance for large-signal phenomena like the negative resistance generated by non-linear capacitors under larger drive levels (parametric effects), as well as gain expansion, can be made by increasing the gain and phase margins derived from small-signal information.

When transistors with strong parametric properties are used, it is crucial to explore the stability at different drive levels too. This is usually done by exploring the response to a small-signal injected into the circuit when it is driven by a strong pump signal. In [3], the stability of a power amplifier (accurate large-signal model required) is examined with a small signal ($f_0/2$; even and odd mode excitation) injected into the combination section when the amplifier is driven by a strong passband signal (f_0). The two signals must be synchronized. Refer to [4] for a review of the different options available for ensuring large-signal stability.

Examples of the start-up odd-mode and even-mode loop gain calculated for an amplifier stage are provided in Figure 7. The loop gain calculated for an oscillator is shown in Figure 8.

Negative resistance in a loop is indicated in the ADW with red segments at the 0 dB gain level (see Figure 8). Without negative resistance at start-up (gain not compressed yet), oscillations are not possible (assuming no gain expansion). Opposite signs in the open loop and feedback reactance are indicated with ticks on these segments (resonance is required at steady state).

Note that the feedback loop is not broken in the ADW when the loop gain is calculated.

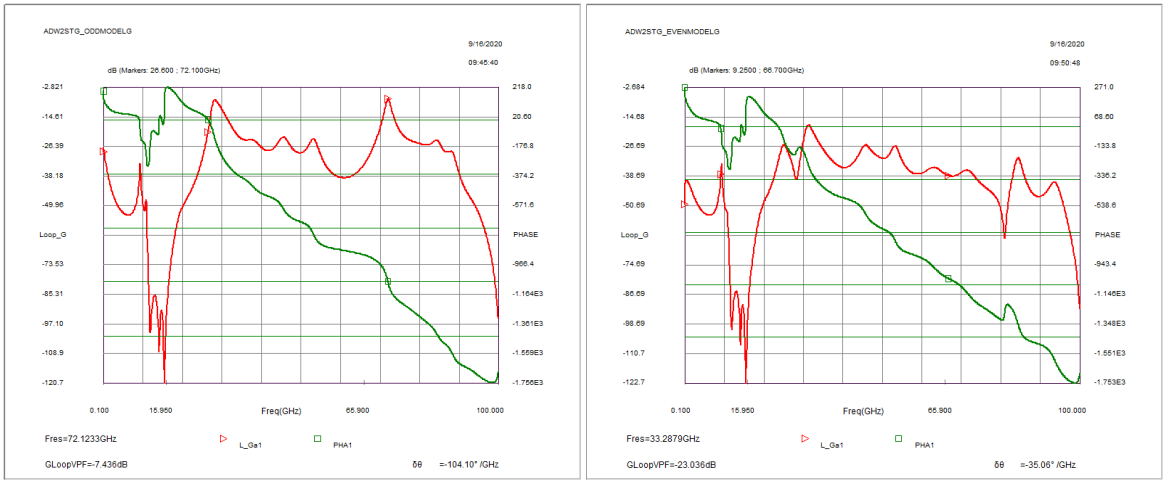


Figure 7. The start-up odd-mode and even-mode voltage-shunt feedback loop gain calculated for a symmetrical transistor combining section in an amplifier. The two sections combined were compensated to be inherently stable before they were combined. Note that the effective resistance in the loop is positive at all frequencies considered.

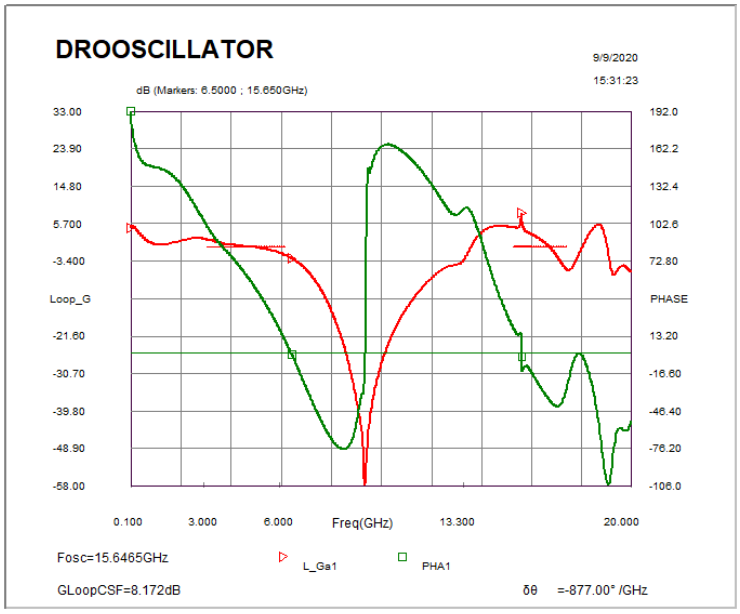


Figure 8. The current-series feedback loop gain calculated for an oscillator in the ADW. Negative resistance is present in two bands in this example. Oscillation in the lower band was suppressed by introducing sufficient margins in the gain and phase with a compensation network.

References

[1] Edwards M.L., and Sinsky J.H., "A New Criterion for Linear 2-Port Stability Using a Single Geometrically Derived Parameter", IEEE Trans. Microwave Theory Tech., Vol. MTT-40, No. 12, December 1992.

[2] Pieter L.D. Abrie, Design of RF and Microwave Amplifiers and Oscillators, Boston: Artech House, Inc. 1999.

[3] Elad, D., Shaulsky, R., Mezhebovsky, B., “A Novel Method for Even Odd Parametric Oscillation Stability Analysis of a Microwave Power Amplifier”, 2006 IEEE MTT-S International Symposium Digest.

[4] Edwards, M., “A review of amplifier stability analysis using modern EDA tools”, ARMMS November 2012.

