Introduction to Designing Doherty Amplifiers with The Ampsa ADW

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Designing a Doherty or Doherty-like amplifier usually reduces to designing the main amplifier to provide the performance required at the medium (transition) and peak power levels and designing the auxiliary amplifier to provide the required performance at peak power and not to load the main amplifier in its off state [1]. These tasks can be performed efficiently in the ADW. Microwave Office™ or ADS™ is required to assemble the designed amplifiers and to adjust the circuit for optimum performance. EM simulation and optimization of the matching networks are generally required. Sonnet®, Axiem™ or Momentum™ can be used to perform these tasks. This process will be reviewed here.

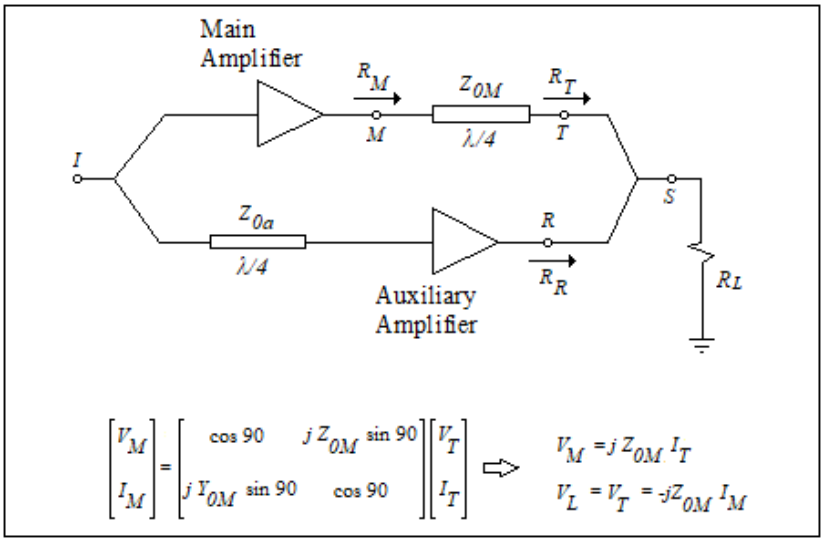

Figure 1. The basic Doherty topology.

The topology for a basic Doherty Amplifier is shown in Figure 1 [2]. The main amplifier is typically biased in Class-AB mode, while the auxiliary amplifier is operated in Class-C mode.

The auxiliary amplifier is biased to turn on when the output voltage of the main amplifier has saturated (medium power level; transition point). The current of the auxiliary amplifier then starts to modulate (increase) the load impedance presented to the main amplifier branch ($Z_T = V_T/I_T = (1+I_R/I_T)\, R_L$). The transmission line (Z_{0M}) serves to invert this increase to allow more power to be extracted from the voltage-saturated main amplifier ($P=V_M^2 / R_M$).

If the amplifiers in Figure 1 are identical and $Z_{0M} = 2R_L$, Z_{0M} will have no transforming effect at peak power. The load impedance presented to both amplifiers will be $2R_L$ and identical load matching networks can be used for the two amplifiers.

At the medium power point (transition point), the auxiliary amplifier is off and should (ideally) present an open at node *R*. R_L is then transformed upwards to 4 R_L at node *M* by Z_{0M}.

Assuming the same voltage (saturated voltage of each amplifier) at node *M*, the backed-off output power will be 6 dBm below the peak output power.

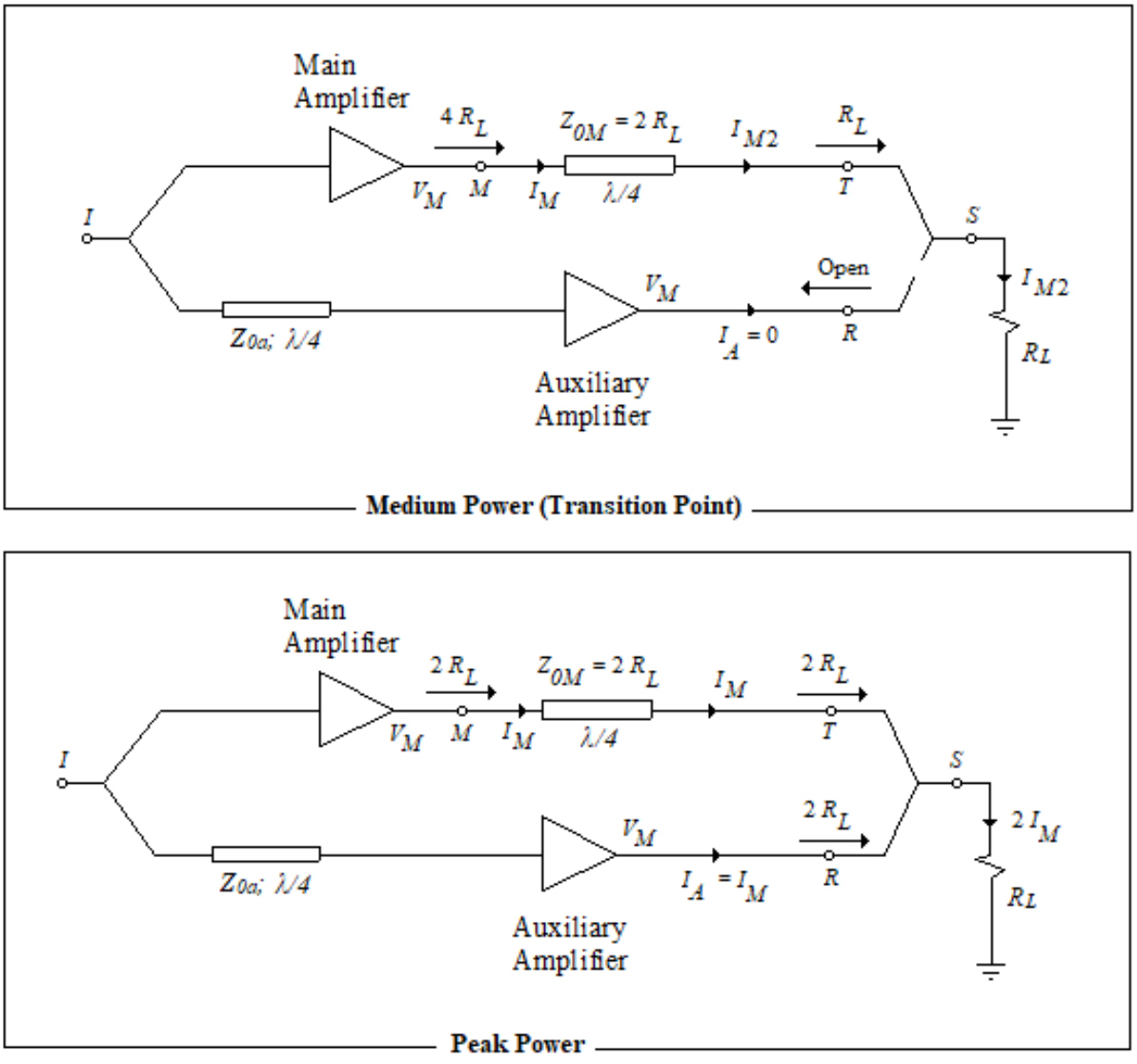

Figure 2. The matching network for the main amplifier is usually designed to provide the required power at the transition point (medium power) and the peak power point. The auxiliary amplifier is designed to provide the peak power required and to have high output impedance while it is off.

The load matching network for the main amplifier is usually designed to provide the load lines required by the transistor at the transition point and the peak power point. Estimates for the intrinsic load-lines can be calculated easily from the power specifications, the supply voltage and the saturation voltage and/or resistance of the transistor ($P = V_M^2/R_M$). The intrinsic load lines usually differ significantly from the impedance required from the matching network (transistor and package parasitic elements; circuitry between the matching network and the transistor).

The external load impedance required for the peak power is usually determined by load-pull experiments. The load impedance associated with the transition point can be estimated by using the VSWR relationship between the estimated intrinsic load lines [4] carried over to the external terminations associated with the peak and medium power points. Efficiency contours are required to select the point to be targeted on the constant VSWR circle [4].

The design process for the Doherty matching networks is simplified by the mapping provided between the intrinsic and external load lines of a transistor in the ADW. The definitions of the mapping parameters are shown in Figure 3. The power parameters map the intrinsic voltages and the intrinsic output current to the external voltages for any linear embedding network.

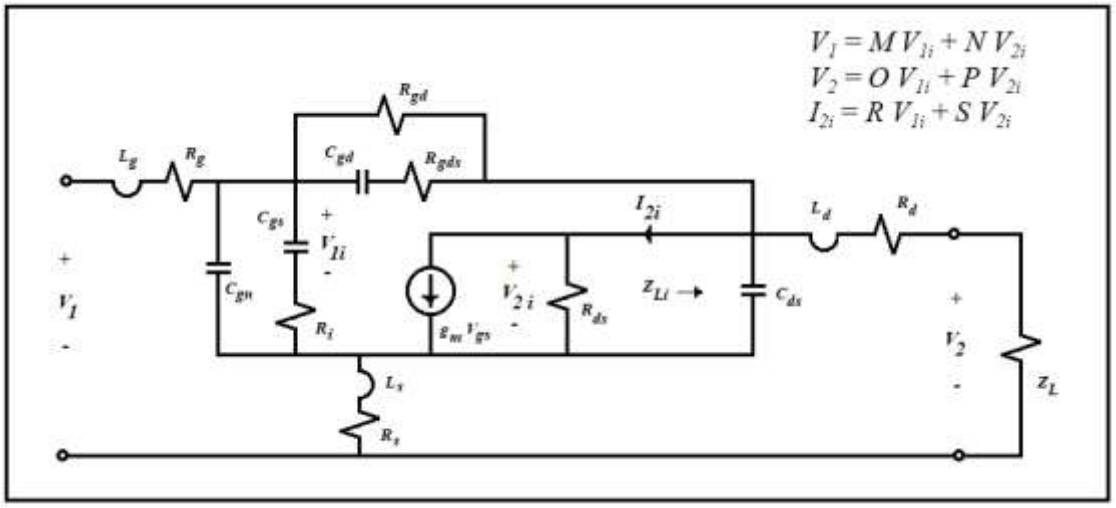

Figure 3. The intrinsic input and output voltages and the intrinsic output current of a transistor can be mapped to the external voltages as shown. The external load associated with any intrinsic load or the intrinsic load associated with any external load can be calculated by using the power parameters.

The power generated by the transistor is determined by the intrinsic load (Z_{Li}). Because of resistive losses in the transistor and feedback effects, the actual output power will not be exactly the same.

Assuming linearity, the external load (Z_L) associated with any intrinsic load or the intrinsic load associated with any external load can be calculated by using the power parameters.

The matching network for the main amplifier should ideally present the transistor with the correct impedance to maximize the efficiency at the peak power level and the medium power level (back-off level), that is the matching network should solve two different (but related) impedance-matching problems at the same time. Fortunately, the load termination for the matching network is also different in each problem because of the Doherty load modulation. (2 R_L versus 4 R_L at the center frequency of the inverting line.)

To get the ADW to find a network that will solve both problems well, the impedance-matching specifications for the medium-power problem can be offset slightly in frequency from those for the peak-power problem, and the two sets of specifications can be combined to create a single set of specifications. (In future versions it will be possible to assign different weights to the two matching problems, but currently the weight factors for the two problems are the same.)

The load terminations required at the peak and medium power points can be found easily by using the CIL Wizard. As an example, the load lines required at 1.64GHz for the Cree CGH41020 for Class-B operation was calculated by targeting 48.4 dBm (peak maximum unclipped power) and 45.4 dBm (medium power level). (The highest efficiency points on the power contours should be selected as targets.) The load lines selected are shown in Table 1 with the efficiency and the output VSWRs. The input of the transistor was assumed to be conjugately matched when the VSWRs were calculated.

Table 1. Intrinsic and External Class-B Load Lines for a Transistor.

Power (dBm)	Drain Efficiency (%)	Z_{Li} (Ohm)	Z_L (Ohm)	Output VSWR (-)
48.45	65.5	4.23 - j0.25	3.48 - j1.98	2.71
45.35	69.2	9.36 - j0.63	4.0 + j1.32	1.34

C_{gd} set to zero (Unilaterization):

Power (dBm)	Drain Efficiency (%)	Z_{Li} (Ohm)	Z_L (Ohm)	Output VSWR (-)
48.37	66.1	4.23 - j 0.27	3.74 - j2.24	16.93
45.38	71.1	9.56 - j0.32	4.73 + j 1.39	14.48

When the intrinsic load line is 4.23 + *j*0, the external load line is 3.30 – *j*1.86, while 8.46 + *j*0 corresponds to 3.81 + *j*0.83.

Note that while the difference between the intrinsic load impedances is mostly in the resistance, the difference in the external impedances are mostly between the reactance. However, the expected VSWR relationship between the peak power and the medium power external impedances [4] does hold (2.0 versus 2.126; exact correlation is not expected). The VSWRs (VSWR = (1+|Γ|)/(1–|Γ|)) are calculated from the following reflection coefficients [4]:

$$\Gamma_e = (Z_{L\_medium} - Z_{L\_peak})/(Z_{L\_medium}+Z_{L\_peak}^{*}) \quad (1)$$

$$\Gamma_i = (Z_{Li\_medium} - Z_{Li\_peak})/(Z_{Li\_medium}+Z_{Li\_peak}^{*}) \quad (2)$$

The expected output VSWRs for the matching network to be designed (see Table 1 and Figure 4) are not high at all. (High output impedance is required to have the performance of a Doherty amplifier linear from the medium to the peak power point.) However, if C_{gd} is removed from the model of the transistor, the output VSWRs increase dramatically. (The change in the intrinsic and external load lines are relatively small.) This illustrates the importance of having s_{12} negligible for the transistors used in a Doherty amplifier (that is, if possible).

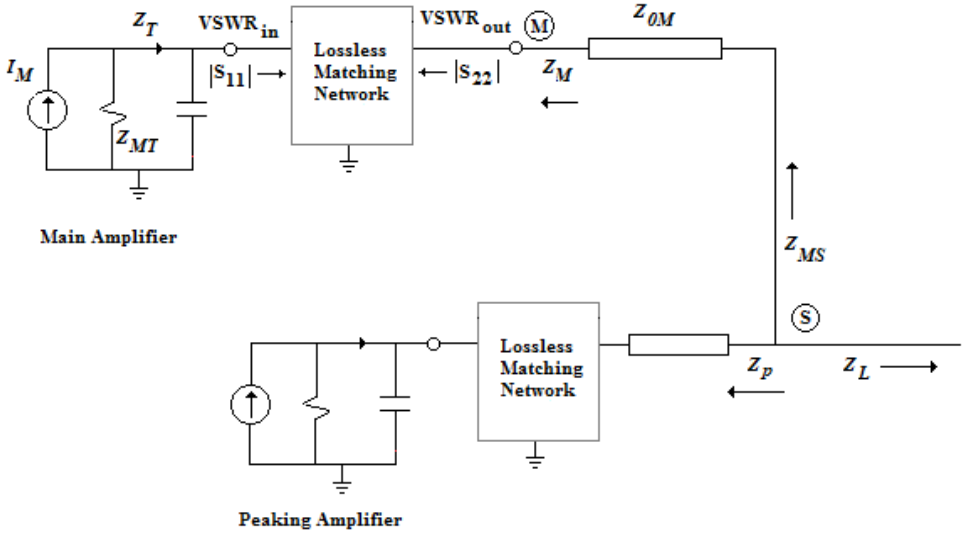

Figure 4. The output VSWR of the lossless matching network ($VSWR_{out}$ above) is set by the VSWR associated with the output impedance of the transistor and load termination presented to it by the matching network ($VSWR_{in}$). If the normalization impedances are the transistor output impedance and the load impedance for the matching network, respectively, $|s_{11}|$ is also equal to $|s_{22}|$.

For lossless load matching networks (refer to Figure 4), the magnitude of the input reflection coefficient, with the transistor output impedance as source (normalization impedance), will be the same as the magnitude of the reflection coefficient on the load side, with the actual load termination for the matching network in place (and used as normalization impedance). It follows from this that the VSWRs on the input side of the lossless matching network will be the same as the VSWRs on the output side.

A high output VSWR for the matching network does not necessarily imply high output impedance at any specific frequency, but the potential of using a transmission line to rotate the impedance to be high does exist. It may also be possible to control the phase of the matching network to assist in getting its output impedance high [5].

If the reverse feedback of the transistor (s_{12}) can be ignored, a shunt inductor can be used to remove the effect of the output capacitance of the transistor at low frequencies, (refer to Figure 5) and, the output resistance will be set mainly by R_{ds}, which is generally high compared to the load impedance required by the transistor (but not necessarily much higher than R_L). The transformers in Figure 5 transform the modulated load impedances downwards to extract the required power from each transistor. The transformers will also transform the output impedances of the transistors upwards, which is desirable.

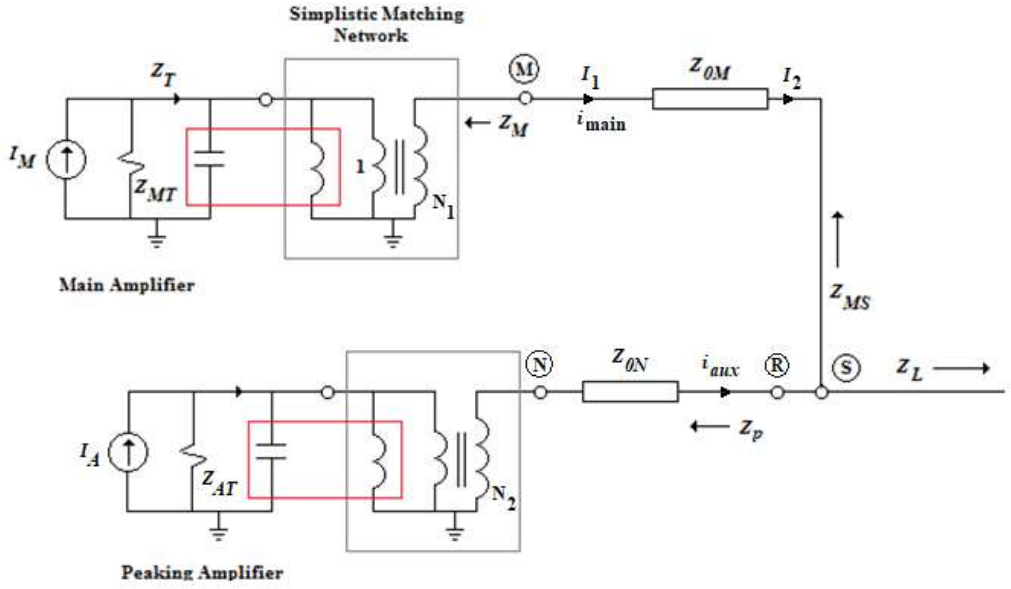

Figure 5. The basic Doherty configuration is shown here with basic models for the transistors and simplistic matching networks.

Note that with the same peak currents for the main and the auxiliary amplifiers, one should aim to get R_L in Figure 5 close to the half of the peak power impedance required.

(This would place less demands on the matching network.) Depending on the impedance levels, this could place unrealistic demands on the characteristic impedance of the transmission lines to be used in the Doherty combination network.

In the ADW, the peak power obtainable from a transistor depends on the boundary set for the maximum current (I_{max} - refer to Figure 6). The optimum terminations at medium power can be established with the model used to establish the peak power load by setting the power required to the back-off level required. The peak-efficiency point on the power contour targeted should then be selected. An alternative approach is to scale I_{max} down to the appropriate level (linear scaling will yield good results). The medium power level will then be the peak power level with the adjusted model.

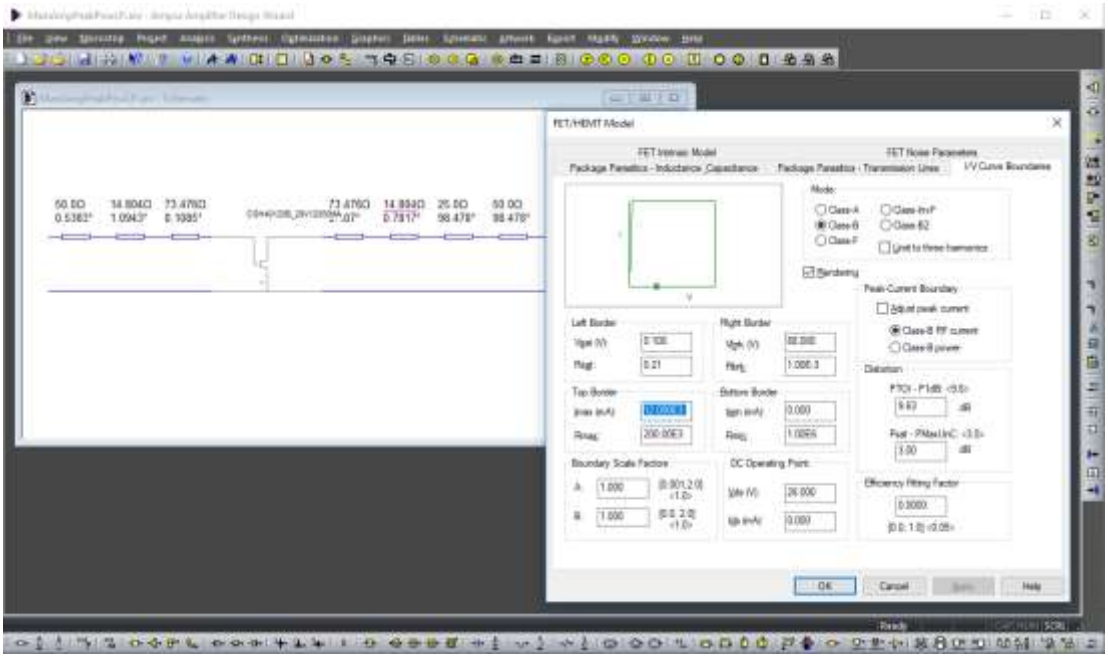

Figure 6. I_{max} (top border) in the ADW transistor model can be scaled down to lower the peak power of the transistor to the medium power level for a Doherty amplifier.

The modulation (gain and phase of the auxiliary amplifier relative to those of the main amplifier) of a Doherty amplifier is designed to keep V_M in Figures 2 or 3 saturated (constant). This will maximize the output power at a given current level and maintain the efficiency. For the modulation to work as designed, the current flowing into the inverting line (I_M) and the current flowing through Node *R* (output current of the auxiliary amplifier) must be linear functions of the input voltage. Given the modulated load terminations in both branches of the amplifier, these requirements can only be met if the output impedances at nodes *M* and *R* are high compared to the modulated impedances at these nodes (current source behavior).

The ratio of the intrinsic drain currents of the main amplifier at the peak and the medium power levels is used as a design parameter in [2]. In this analysis, the definitions are modified: i_{main} is taken to be the current entering the inverter line (Z_{0M}), while i_{aux} is taken to be the current flowing through Node *R* in Figure 5. The ratio of i_{main} at the peak power level and i_{main} at the medium power level (saturated power level with the auxiliary amplifier off) is taken to be the design parameter γ:

$$\gamma = i_{\text{main\_peak}} / i_{\text{main\_medium}} \tag{3}$$

Note that when Z_{MT}, Z_{AT} and the transmission line Z_{0N} can be ignored and $N_1 = 1 = N_2$, i_{main} is I_M and i_{aux} is I_A.

The voltage at Node *M* is assumed to have reached its peak value at the medium power level.

For the output voltage of the main amplifier (voltage at Node *M*) to remain constant from the medium power point to the peak power point, the output current of the auxiliary amplifier (i_{aux}) must track the increase in current of the main amplifier beyond the medium power point as described by the equation shown below:

$$i_{\text{aux}} = -j\,(Z_{0m} / R_L)\,(i_{\text{main}} - i_{\text{main\_medium}}) \tag{4}$$

when

$$i_{\text{main}} > i_{\text{main\_medium}}.$$

The equation shown above is set by the properties of the inverter line Z_{0M} when it is exactly 90° long. At this frequency, a constant input voltage for the line (V_M) is associated with a constant output current ($V_M = j\,Z_{0M}\,I_2$), and the output voltage (V_L) is only a function of the current flowing into the line (I_1 or i_{main}) and the characteristic impedance of the line ($V_L = -j\,Z_{0M}\,i_{\text{main}}$). These properties follow directly from the transmission matrix of the line.

It follows from (4) that the rate of change of i_{aux} must be (Z_{0M} / R_L) times the rate of change of i_{main} for the output voltage of the main amplifier to remain constant beyond the medium power point. The input splitter is usually designed asymmetrically to provide for this difference in the gain. (Also note the 90° phase shift required between the i_{main} and i_{aux}.) Because the relative rate of change for the currents are fixed by the circuit, the maximum current of the auxiliary amplifier is tied to the maximum current of the main amplifier. With

$$\alpha = i_{\text{main}} / i_{\text{main\_peak}} \tag{5}$$

the following equations apply:

$$i_{aux} = -j\,(Z_{0M} / R_L)\,(\alpha - 1/\gamma) \times i_{\text{main\_peak}} \tag{6}$$

$$i_{aux\_peak} = (Z_{0M} / R_L)\,[(\gamma - 1)/\gamma] \times i_{main\_peak} \tag{7}$$

The impedance presented to the main amplifier by the combining circuit and the impedance presented to the auxiliary circuit are also important. The impedance at Node *M* and Node *R* are given by the equations shown below.

$$\begin{aligned} R_{\text{main}} &= Z_{0M}^2 / R_L, \quad i_{\text{main}} \le i_{\text{main\_medium}} \\ &= [Z_{0M}^2 / (\gamma R_L)] / \alpha, \qquad i_{\text{main}} > i_{\text{main\_medium}} \end{aligned} \tag{8}$$

$$R_{aux} = [\alpha\,\gamma\,/\,(\alpha\,\gamma\,-1)]\,R_L, \qquad \alpha > 1/\gamma \tag{9}$$

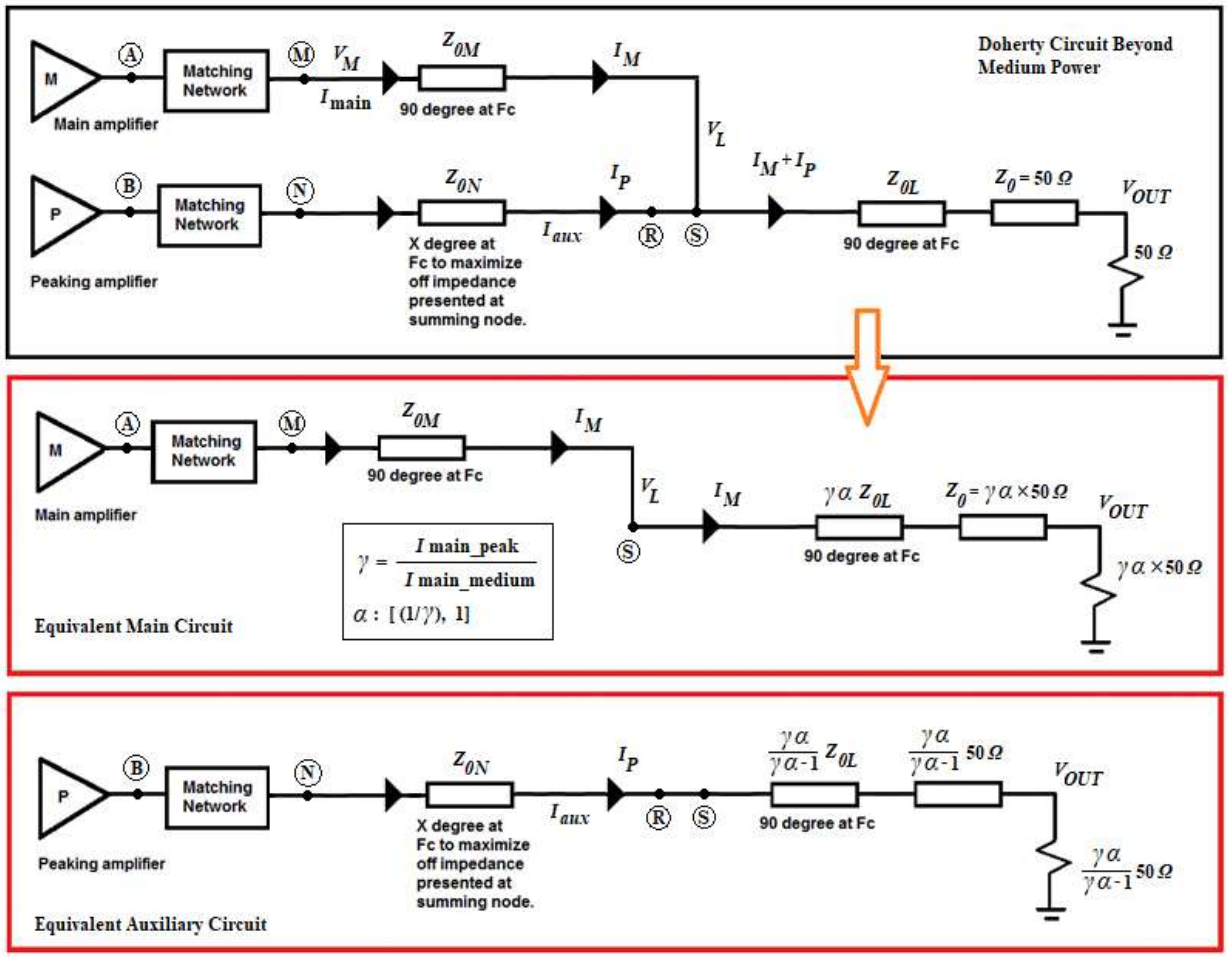

Figure 7. The Doherty design problem can be reduced to designing two separate amplifiers. The approach is illustrated here.

The voltage at Node M is given by

$$V_M = R_{\text{main}}\, i_{\text{main}} = (Z_{0M}^2 / R_L)\, (i_{\text{main\_peak}} / \gamma) \tag{10}$$

The voltage at Node R is given by

$$V_R = R_{\text{aux}}\, i_{\text{aux}} = [\alpha\, \gamma\ / (\alpha\, \gamma\ - 1)]\, R_L\, [-j\, (Z_{0M} / R_L)\, ((\alpha\, \gamma - 1)/ \gamma)] \times i_{\text{main\_peak}}$$

$$= -j\, \alpha\, Z_{0M} \times i_{\text{main\_peak}} \tag{11}$$

For the voltage at Node R (also node N) to have the same peak value as the voltage at Node M, it is required that

$$Z_{0M} / R_L = \gamma \tag{12}$$

If a different (supply) voltage can be used for the auxiliary amplifier

$$\gamma = (Z_{0M} / R_L)\, (V_R/V_M) \tag{13}$$

The output power of the Doherty amplifier at the center frequency is given by

$$P_{\text{out}} = V_L^2/R_L = (Z_{0M}^2/R_L) \times i_{\text{main}}^2 = (Z_{0M}^2/R_L) \times i_{\text{main\_max}}^2 \times \alpha^2 \tag{14}$$

The peak to medium power ratio of the Doherty amplifier is equal to γ^2.

If the current tracking between the main and the auxiliary amplifiers are assumed to be perfect, the Doherty design problem can be reduced to designing two cascade amplifiers as shown in Figure 7. The designed amplifiers can then be combined, and the performance can be optimized.

Note that when γ is equal to 2 (6 dBm back-off at medium power) and $Z_{0M} = 2R_L$, the peak currents of the two amplifiers will be the same (see Equation 6) and the load-lines at peak power ($2R_L$) will also be the same (refer to Equations 8 and 9). It is not possible to have the load lines the same over the whole medium to peak power range.

The main amplifier and the auxiliary amplifier can be identical when $\gamma = 2$ and $Z_{0M} = 2R_L$. Because of the difference in the load-lines required by the two amplifiers in the medium power to peak power range, the Doherty condition for constant V_M cannot be satisfied perfectly. The design is usually done to satisfy the conditions at the medium and the peak power points.

In Figure 5, matching for either the medium or the peak power level will be adequate. The load lines for the two power levels differ by a factor γ and with the voltage (almost)

constant from the medium to the peak power level, satisfying one of the conditions will also satisfy the other condition.

The recommended approach for designing a Doherty amplifier with the ADW as follows:

1. The peak power and the back-off power specifications will establish the γ-value ($\gamma^2 = P_{out\_peak} / P_{out\_backoff}$) and the supply voltage(s) will set the value of Z_{0M} (Equation (12) or (13)).

   Note that it is generally a good idea to transform the load impedance downwards to present a low impedance at the summing node of the combiner (Node *S* in Figure 7). The lowest impedance is set by realistic values for the characteristic impedance of the lines used in the combining structure and the intrinsic load terminations required by the transistors. Greater flexibility is provided when a hybrid coupler instead of the standard Doherty combiner is used [3].

2. Design a matching network to control the power of the main amplifier at the medium and the peak levels. The Power Contours option provided in the CIL wizard can be used to set up the specifications for each of the two matching problems. Select the highest efficiency point on each contour.

   The two matching problems can be combined to design a single matching network to solve both problems. The networks defining the load terminations to be used for the two problems are shown in Figure 7 (Equivalent circuit to the right of Node *M;* $\alpha = 1/\gamma$ and α=1).

   The output impedance of the matching network designed should ideally also be high when it is terminated on its input side in the output impedance of the transistor.

3. If the peak power required from the auxiliary amplifier is not the same as that of the main amplifier, design this amplifier to provide the peak power required. The output impedance of the matching network designed should ideally also be high when it is terminated on its input side in the output impedance of the transistor.

   Transmission line Z_{0N} in Figure 7 can be used to rotate the output impedance of the auxiliary amplifier to be high in its off-state. This is necessary to prevent loading of the main amplifier path by the auxiliary amplifier when it is off.

4. Export the matching networks and the combining network and set up the amplifier for analysis and optimization in Microwave Office™ or ADS™. An asymmetrical splitter can be used on the input side of the amplifier to increase that gain in the

auxiliary amplifier branch as required (refer to Equation 6). A transmission line is also required at the input of the auxiliary amplifier to establish the phase relationship required between i_{main} and i_{aux}.

Step 2 is illustrated in Figure 8 and 10.

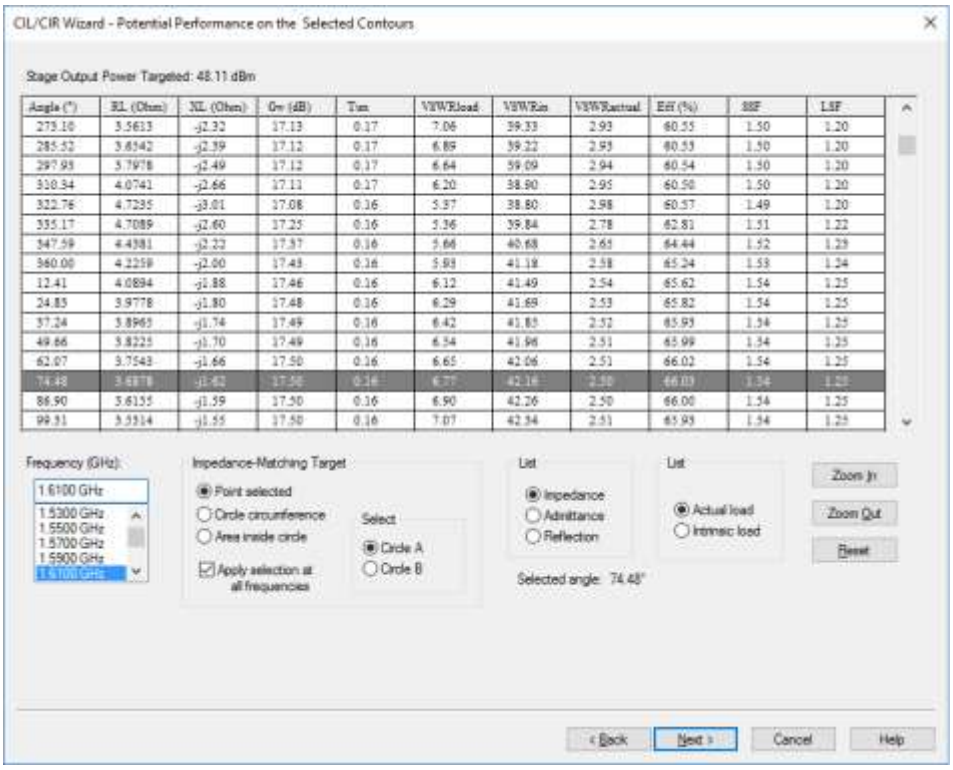

Figure 8. The point to be targeted on a constant power contour can be selected in the ADW. The highest efficiency point is usually targeted, but if the loss in efficiency is acceptable, a point with higher $VSWR_{actual}$ (the output VSWR expected with the transistor and the matching network in place) can be selected.

The data defined by two separate matching problems (".mmi" files) were merged in Figure 9. The merging can be done by following the steps shown below.

1. Open the data file for the peak power problem. Then use File | Save As to change the file name.

2. Import the data associated with the medium power problem by using the File | Import command.

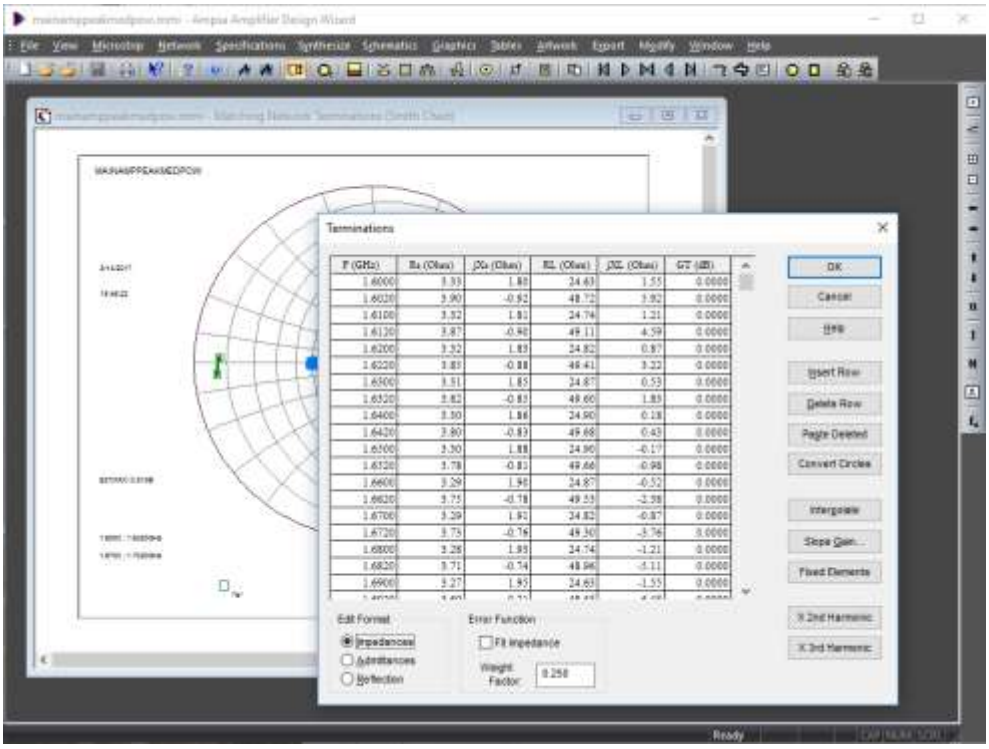

Figure 9. The ADW fundamental-frequency specifications for the load matching network of a Doherty amplifier are shown here. A frequency offset of 2MHz was used for the medium power matching problem. Note that the conjugates of the input impedance required from the matching network are specified here.

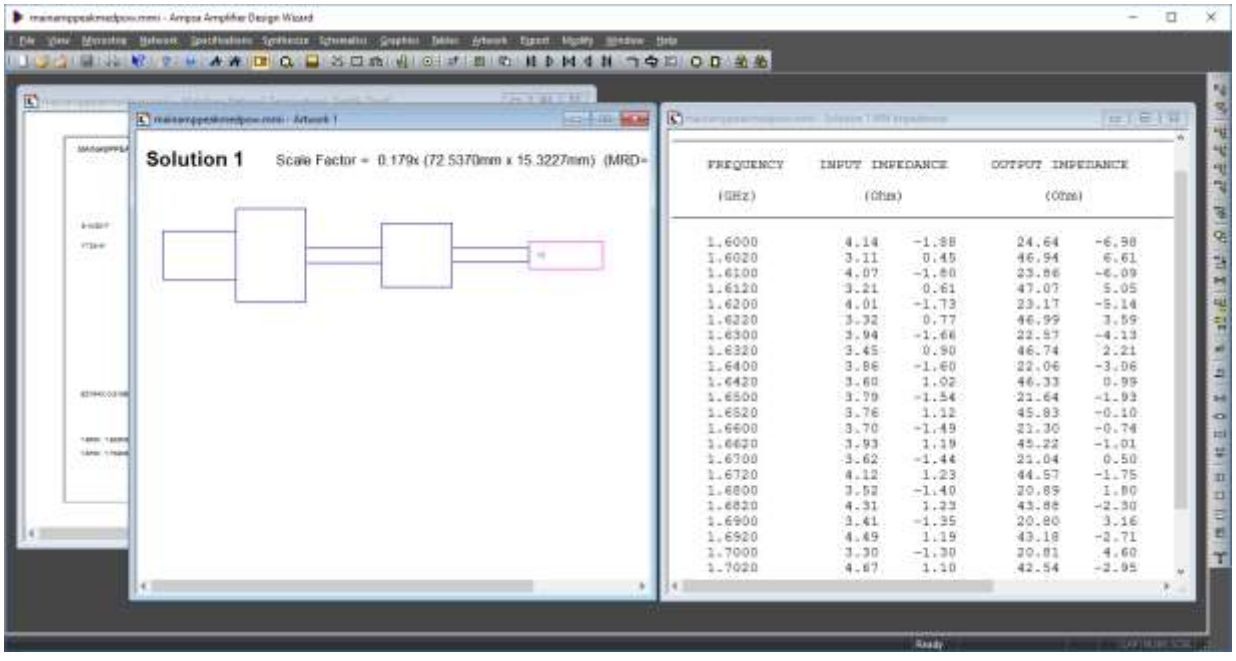

Figure 10. The input impedance associated with a solution to Doherty matching problem is listed here.

With the data set up correctly, solutions were synthesized to the combined problem. The solution selected was then exported as an ADW circuit file, after which it was adjusted by introducing extra steps in the network to reduce the discontinuity effects associated with the large steps in the solution. The adjusted matching network was then optimized to restore it.

The artwork of the solution should be exported to an EM simulator to verify that its performance is close to the desired electrical performance. Adjustments should be made to the artwork if necessary. This was done in this example and artwork was optimized by using the Reverse Update feature provided in the ADW. The artwork before and after the adjustments is shown in Figure 11.

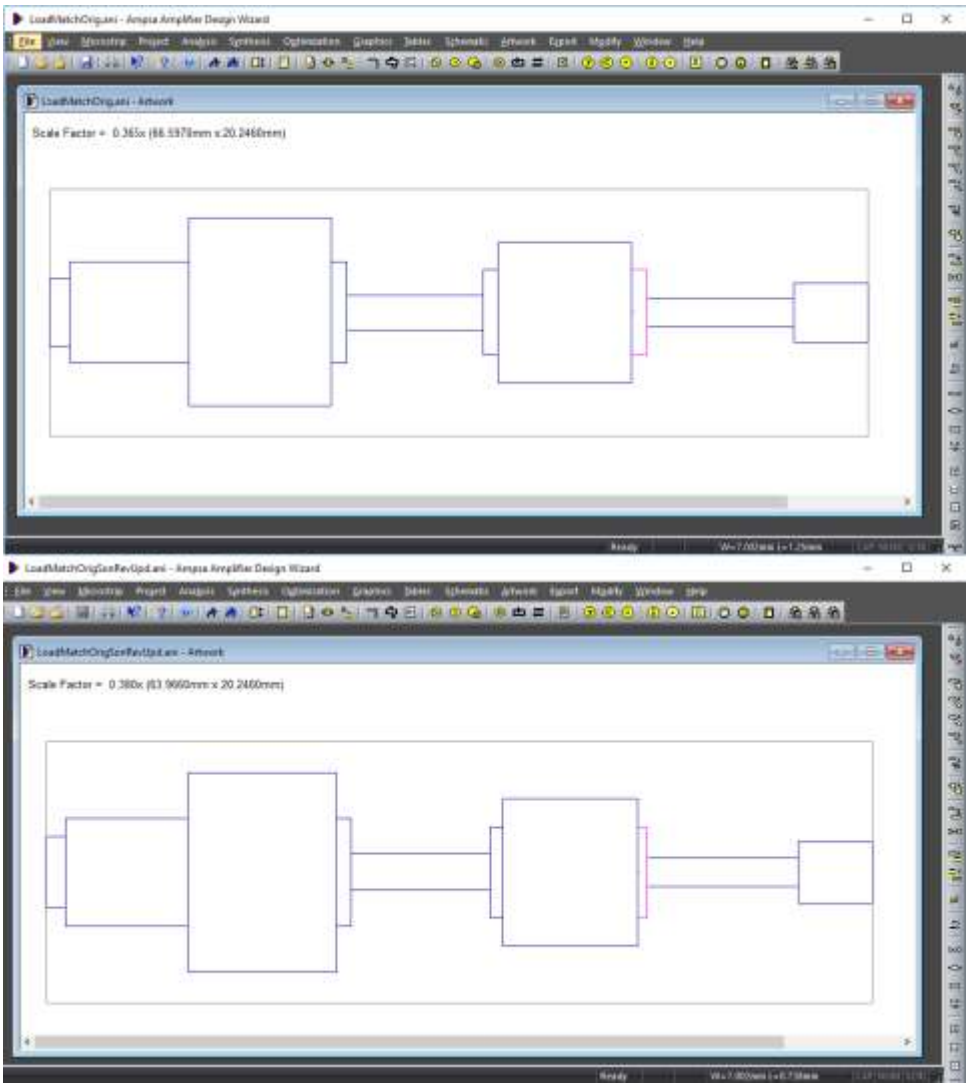

Figure 11. The artwork of the matching network was adjusted by using the Reverse Update optimization feature provided in the ADW.

The steps in the Reverse Update procedure are summarized below.

1. Export the artwork of the ADW solution for EM simulation. (Sonnet® was used in this example). Export a set of two-port *S*-parameters for the EM simulation.

2. Import the *S*-parameters obtained from the EM simulation into the ADW circuit file.

3. Mark the variables to be optimized by using the Optimize Element command provided on the Schematic Editing Toolbar. The Optimization Bounds command can be used to set bounds for any of the variables marked.
   Selecting only the lines lengths for optimization are usually adequate.

4. Use the Model Optimization Error Function command provided on the Program Toolbar to select the two-port *S*-parameter file associated with the EM simulation as target for the optimization. Select the L_1 and *S*-parameters options for the optimization.

5. Use the Optimization command provided on the Program Toolbar to optimize the circuit. The option to update the circuit variables to the optimized values will be provided. Select the Reverse Update option provided.

6. Save the circuit and export the artwork for re-simulation in the EM simulator. The performance should now be close to the electrical performance of the ADW circuit before the optimization. (Note that the electrical circuit is analyzed in the ADW and not the artwork.)

Note that after the Reverse-Update adjustments, it does not make sense to simulate the circuit in the ADW. The modified network should be simulated in the EM simulator to verify its performance and the *S*-parameters associated with this simulation can be used in the ADW instead. An alternative to using the Reverse-Update feature is to simulate the junctions in the ADW circuit in an EM simulator and to use the EM *S*-parameters to model these junctions in the ADW (recommended approach).

While the transistor selected cannot provide the high output impedance required for ideal Doherty operation, the design for the main amplifier was completed as shown in Figure 12. Two versions of the main amplifier were designed. The first version was only designed to provide a good match on the input side (at both the medium and the peak power levels), while a modification network was used in the second design to stabilize the transistor and to level the gain in addition to providing a good match on the input side. Note that 3.5 dB in gain was lost in the process of doing this. However, the amplifier is overly stable and some of the loss can be regained by lowering the stability margins.

The main amplifier without the stabilization networks was then used to assemble the amplifier in Microwave Office™. A quadrature hybrid was used to split the input signal to the main and the auxiliary amplifiers. For best performance the coupling factor was reduced to 1.8 dB. A line was also added to adjust the phase in the auxiliary amplifier path

(12° at 1700MHz). An asymmetrical splitter with a phase line can be designed to replace the quadrature hybrid, if necessary.

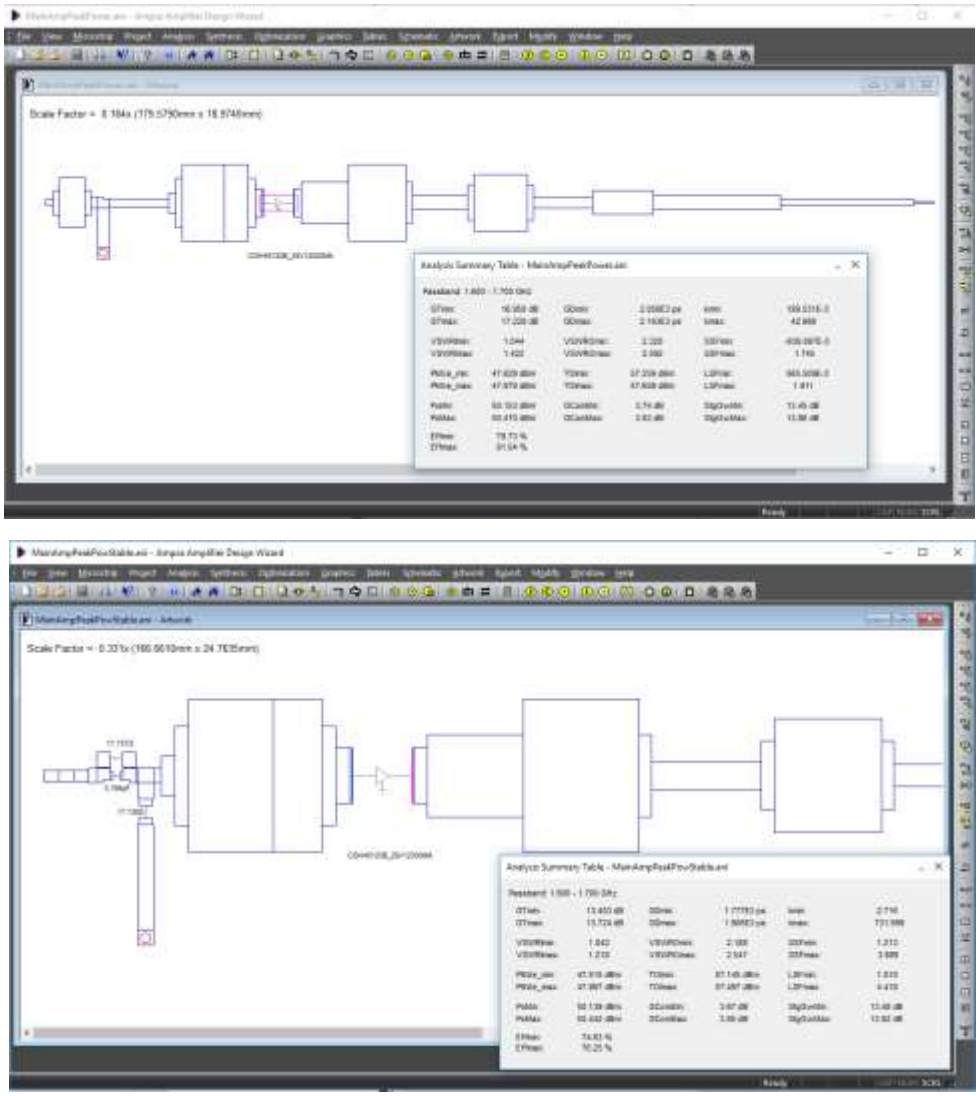

Figure 12. The main amplifier designed is shown here with and without stabilization. The same load network was used in the two amplifiers.

With the quadrature hybrid used, the coupling factor of 1.8 dB implies more signal for the main amplifier than the auxiliary amplifier (Not quite Doherty behavior. In a Doherty amplifier more gain is required for the auxiliary amplifier to keep the voltage V_M constant - V_M is not required to be constant in this amplifier. The lower gain associated with Class-C operation also increases the demand for gain in a Doherty amplifier.)

The performance of the amplifier at 1650 MHz, as simulated in Microwave Office™, is shown in Figure 13. Reverse-updated versions of the load and input matching networks were exported to Microwave Office™ for the simulation.

Some of the line widths and step sizes were out of range (X-models) in the Microwave Office™ simulation and because of this, Axiem™ should be used to simulate sections of the design. However, this example mainly serves to demonstrate a design flow and it was decided to evaluate the performance of the ADW electrical design (instead of the microstrip design) in Microwave Office™. (The discrepancies between the electrical and microstrip designs can be eliminated or reduced by EM simulations or EM optimization of the matching networks.) The bias voltage for the auxiliary amplifier, the coupling factor of the hybrid splitter and the electrical length of the extra line added were adjusted to fine-tune the performance (refer to Figure 14; swept variables were used to fine-tune the circuit). The performance is shown in Figures 15, 16 and 17.

It is clear from Figures 13 and 15 that performance of the electrical network is better than that of the other network. (Note that the gain compression is also less). The optimum parameters for the quadrature hybrid are also different.

The gain compression from the small-signal level (P_{in}=10 dBm) to the P_{out}=53 dBm power level is 2.9, 3.4 and 3.5 dB at 1600 MHz, 1650 MHz and 1700MHz, respectively.

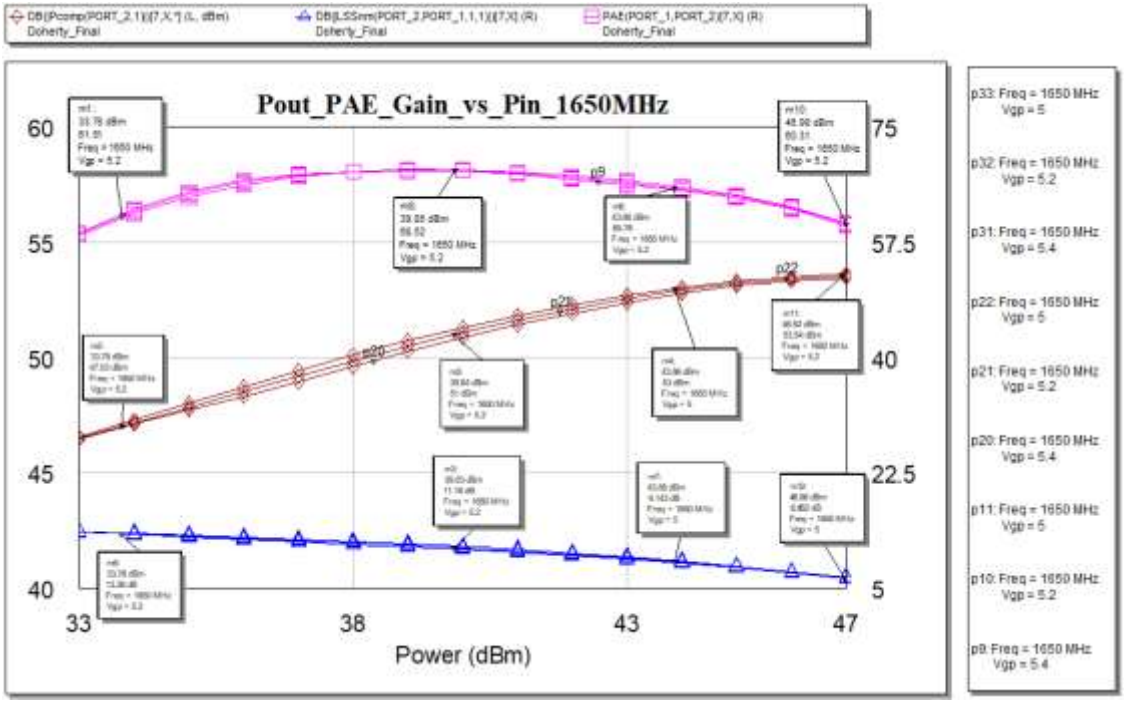

Figure 13. The output power, the power-added efficiency and the gain of the amplifier, as simulated in Microwave Office™, are shown here. The Class-C gate voltage for the transistor in the auxiliary amplifier was set to 5.0V, 5.2V and 5.4V.

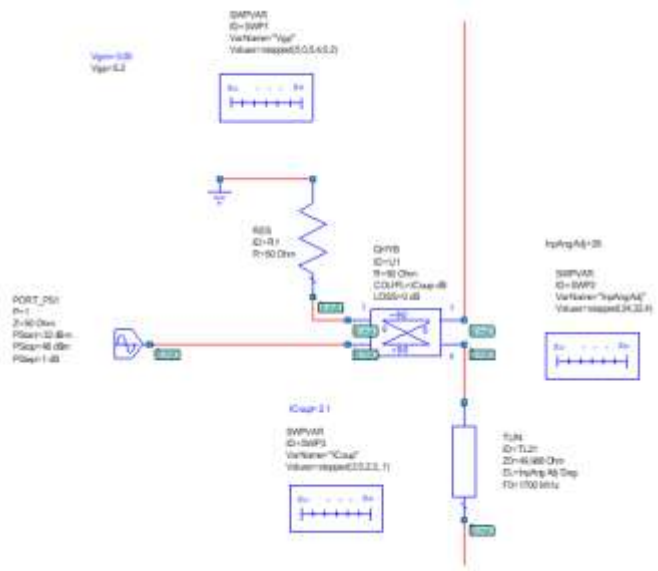

Figure 14. A quadrature hybrid with a 2.1 dB coupling factor was used to split the input signal for the amplifier assembled in Microwave Office™ (ADW electrical design). The 90° phase shift associated with the quadrature hybrid was adjusted by using the 28° line shown.

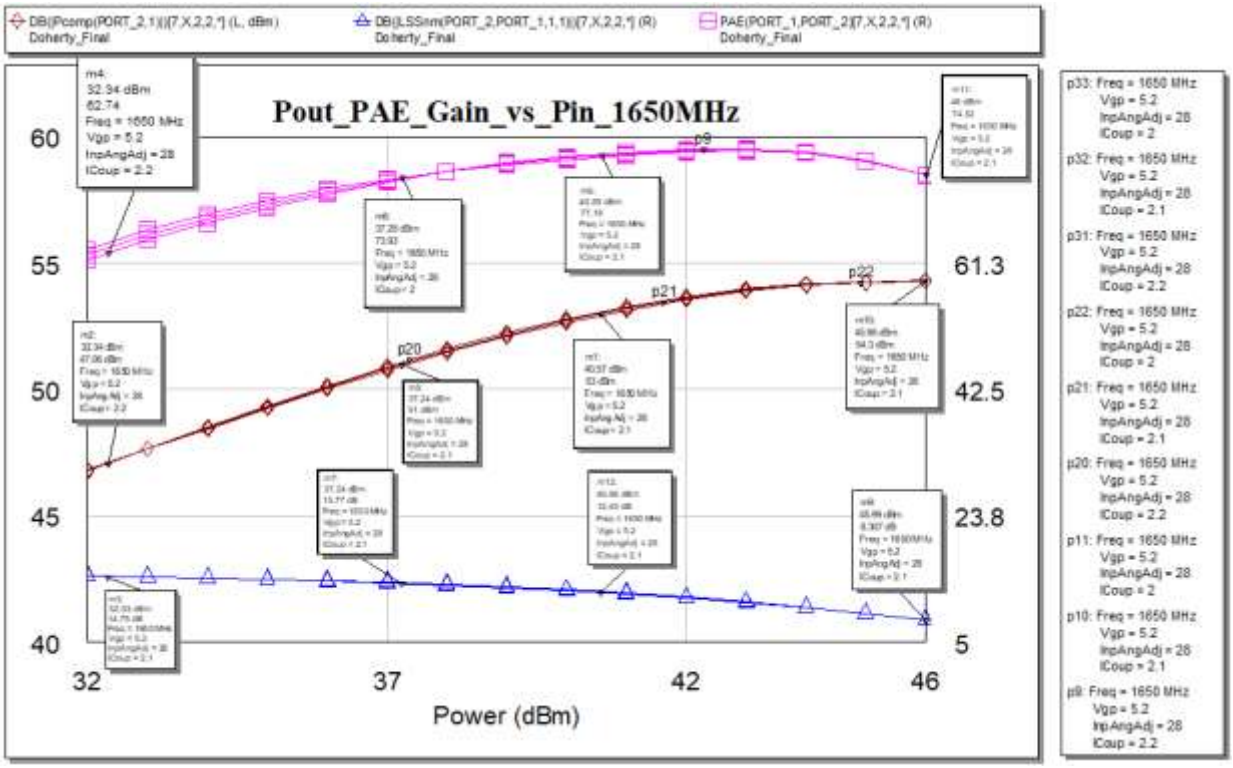

Figure 15. The output power, the power-added efficiency and the gain of the amplifier (ADW electrical design) at 1650 MHz are shown here.

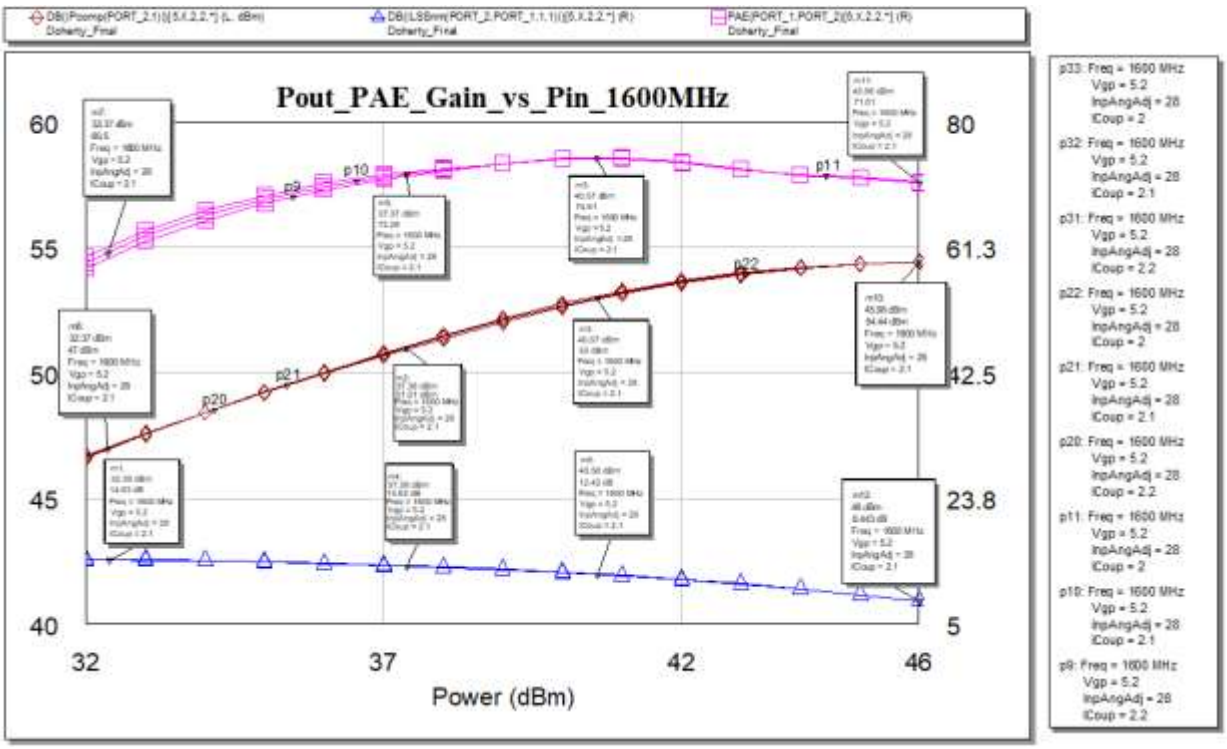

Figure 16. The output power, the power-added efficiency and the gain of the amplifier (ADW electrical design) at 1600 MHz are shown here.

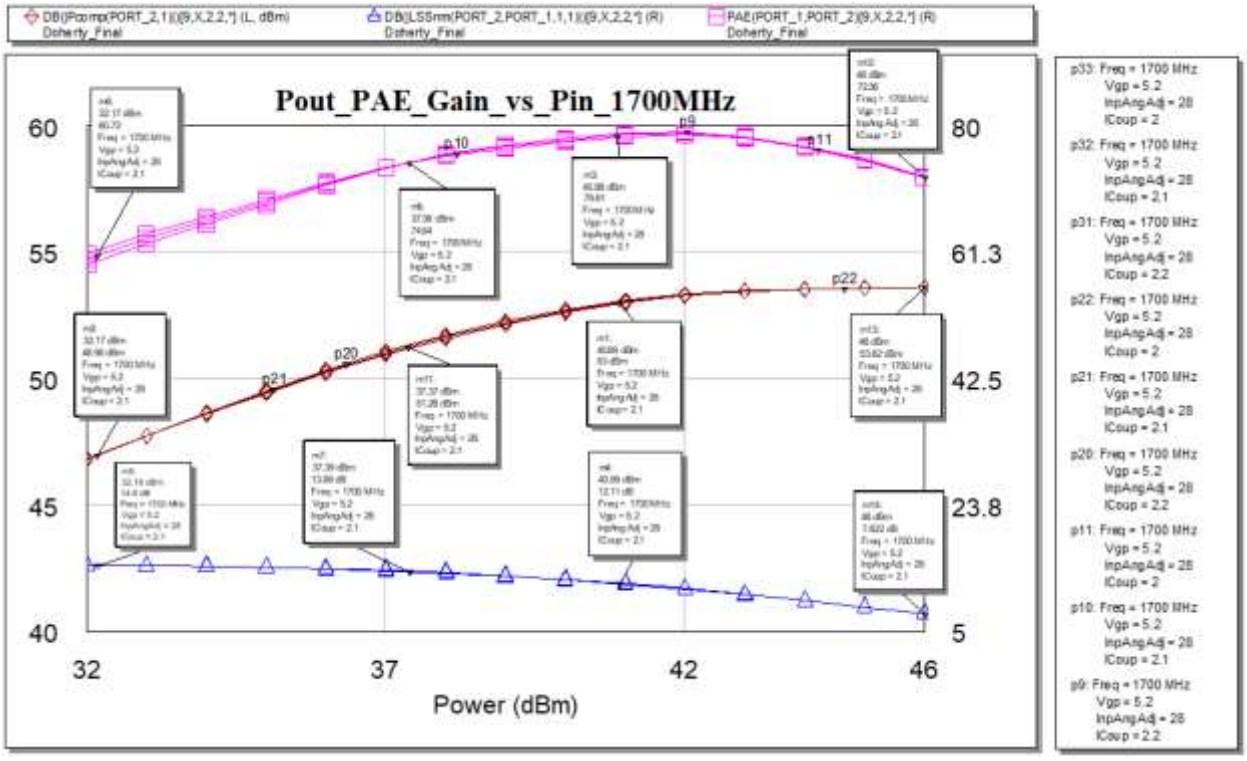

Figure 17. The output power, the power-added efficiency and the gain of the amplifier (ADW electrical design) at 1700 MHz are shown here.

The main issue in porting an ADW design to a harmonic-balance simulator is usually not the differences between the linear simulation in the ADW and the non-linear simulation in the harmonic-balance simulator. The differences in the microstrip (and other) models are usually more important.

It is highly advisable to extract the main matching networks, modifications networks and combinations networks as separate circuits from the ADW design and to optimize the artwork of each of these circuits to provide the electrical performance required.

The ADW *S*-parameters associated with each of these sub-circuits should be exported as a Touchstone ".s2p" file (ADW Export | Touchstone *S*-parameter file menu command) and can be used as targets to adjust the artwork (the frequency range for the fit must often include the harmonic frequencies too). The required adjustments can be made in the ADW (external EM simulation is required), in an EM simulator or in the harmonic-balance simulator to be used. Adjusting the artwork of each passive network is a linear process and can usually be done quickly. Because the simulation speed is not an issue, the networks can often be adjusted by tuning the network elements in the simulator used.

The process described is much faster than trying to optimize the complete ADW network in the harmonic-balance simulator. The simulation time in the harmonic-balance simulator is frequently an issue (especially if more than one transistor is used) and there is also the problem of local minima.

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